THE μCOM87 FAMILY

DATA-BOOK

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8-BIT SINGLE CHIP MICROCOMPUTER

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PRODUCT	PACKAGE	ROM RAM	INSTRUCTIONS I/O LINES	INTERRUPTS – EXTERNAL – INTERNAL	SPECIAL FEATURES
μPD7800	64 QUIL	– 128	140 48	3 2	EVACHIP FOR μPD7801/02
μPD7801	64 QUIL	4096 128	140 48	3 2	
μPD7802	64 QUIL	6144 64	140 48	3 2	
μPD78C05A	64 QUIL	– 128	101 46	2 1	EVACHIP FOR μPD78C06A CMOS-TECHNOLOGY
μPD78C06A	64 FLAT 64 QUIL	4096 128	101 46	2 1	CMOS
μPD7807	64 QUIL 64 SDIP	– 256	157 40	3 8	EVACHIP FOR μPD7809
μPD7808	64 QUIL 64 SDIP	4096 256	157 40	3 8	4K VERSION OF 7809
μPD7809	64 QUIL 64 SDIP	8192 256	157 40	3 8	8 COMPARATOR INPUTS, TWO 8-BIT TIMERS, ONE 16-BIT TIMER / COUNTER
μPD78P09	64 QUIL	8192 256	157 40	3 8	EPROM-VERSION OF μPD7809
μPD7810	64 QUIL 64 SDIP	– 256	157 44	3 8	EVACHIP FOR μPD7811
μPD7811	64 QUIL 64 SDIP	4096 256	157 44	3 8	8 A/D-CONVERTER INPUTS, TWO 8-BIT TIMERS, ONE 16-BIT TIMER / COUNTER
μPD78PG11E	64 QUIL	4096 256	157 44	3 8	PIGGY BACK VERSION OF μPD7811
μPD7810H	64 QUIL 64 SDIP	– 256	157 44	3 8	HIGH SPEED VERSION OF μPD7810 (15 MH_Z)
μPD7811H	64 QUIL 64 SDIP	4096 256	157 44	3 8	HIGH SPEED VERSION OF μPD7811 (15 MH_Z)
μPD78C10	64 QUIL 64 FLAT 64 SDIP	– 256	158 44	3 8	CMOS VERSION OF μPD7810
μPD78C11	64 QUIL 64 FLAT 64 SDIP	4096 256	158 44	3 8	CMOS VERSION OF μPD7811
μPD78C14	64 QUIL 64 FLAT 64 SDIP	16384 256	158 44	3 8	CMOS VERSION OF μPD7811

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HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER ROM-LESS DEVELOPMENT DEVICE

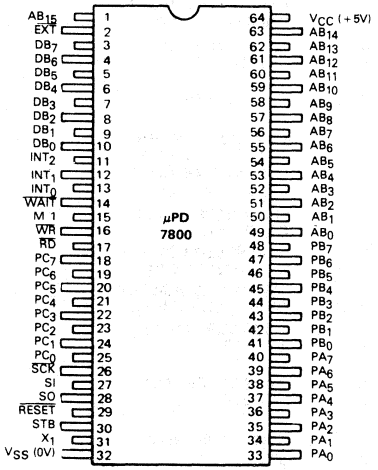
DESCRIPTION

The NEC μPD7800 is an advanced 8-bit general purpose single-chip microcomputer fabricated with N-channel Silicon Gate MOS Technology. Intended as a ROM-less development device for NEC μPD7801/7802 designs, the μPD7800 can also be used as a powerful microprocessor in volume production enabling program memory flexibility. Basic on-chip functional blocks include 128 bytes of RAM data memory, 8-bit ALU, 16-bit adress bus, 32 I/O lines, Serial I/O port, and 12-bit timer. Fully compatible with the industry standard 8080A bus structure, expanded system operation can be easily implemented using any of 8080A/8085A peripheral and memory products. Total memory address space is 64K bytes.

FEATURES

- NMOS Silicon Gate Technology Requiring Single +5V Supply
- Single-Chip Microcomputer with On-Chip ALU, RAM and I/O
  - 128 Bytes RAM
  - 32 I/O Lines
- Internal 12-Bit Programmable Timer
- On-Chip 1 MHz Serial Port
- Five-Level Vectored, Prioritized Interrupt Structure
  - Serial Port
  - Timer
  - 3 External Interrupts
- Bus Expansion Capabilities
  - Fully 8080A Bus Compatible
  - 64K Byte Memory Address Range
- Wait State Capability
- Alternate Z80™ Type Register Set
- 140 powerful instructions
- 8 Address Modes; Including Auto-Increment/Decrement
- Multi-Level Stack-Capabilities
- Fast 2 μs Cycle Time
- Bus Sharing Capabilities (DMA)

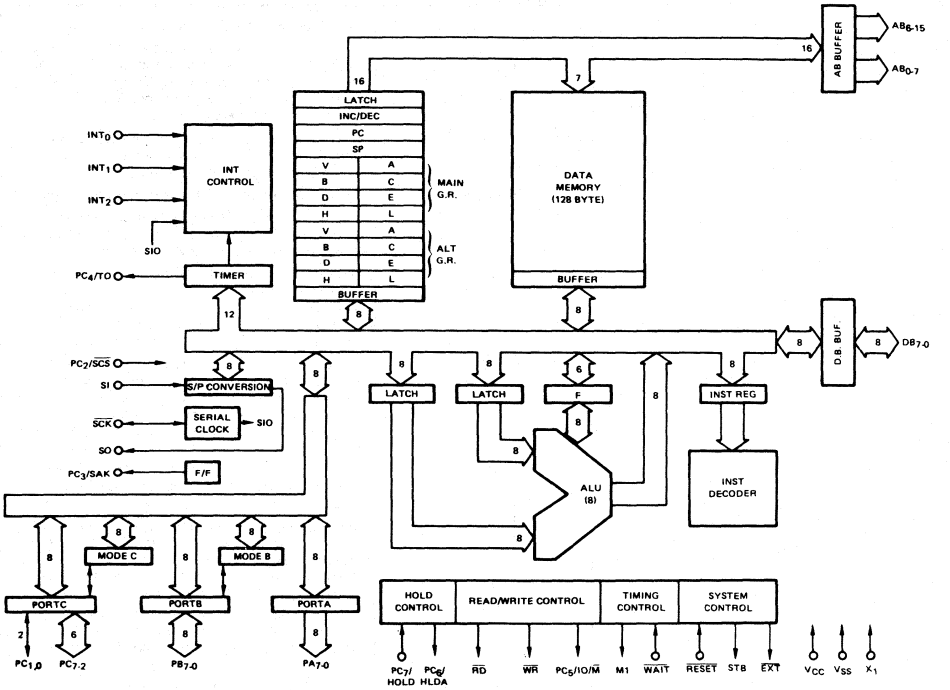
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	DESIGNATION	FUNCTION
1, 49-63	AB_0-AB_{15}	(Tri-State, Output) 16-bit address bus.
2	$\overline{EXT}$	(Output) $\overline{EXT}$ is used to simulate μPD7801/7802 external memory reference operation. $\overline{EXT}$ distinguishes between internal and external memory references, and goes low when locations 4096 through 65407 are accessed.
3-10	DB_0-DB_7	(Tri-State Input/Output, active high) 8-bit true bi-directional data bus used for external data exchanges with I/O and memory.
11	INT_0	(Input, active high) Level-sensitive interrupt input.
12	INT_1	(Input, active high) Rising-edge sensitive interrupt input. Interrupts are initiated on low-to-high transitions, providing interrupts are enabled.
13	INT_2	(Input) INT_2 is an edge sensitive interrupt input where the desired activation transition is programmable. By setting the ES bit in the Mask Register to a 1, INT_2 is rising edge sensitive. When ES is set to 0, INT_2 is falling edge sensitive.
14	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state TW and remains in that state as long as $\overline{WAIT}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices on the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-25	PC_0-PC_7	(Input/Output) 8-bit I/O configured as a nibble I/O port or as control lines.
26	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of $\overline{SCK}$.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of $\overline{SCK}$, MSB to LSB.
29	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD7800.
30	STB	(Output) Used to simulate μPD7801/7802 Port E operation, indicating that a Port E operation is being performed when active.
31	X_1	(Input) Clock Input
33-40	PA_0-PA_7	(Output) 8-bit output port with latch capability.
41-48	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Architecturally consistent with μPD7801/7802 devices, the μPD7800 uses a slightly different pin-out to accommodate for the address bus and lack of on-chip clock generator. For complete μPD7800 functional operation, please refer to μPD7801 product information. Listed below are functional differences that exist between μPD7800 and μPD7801 devices.

μPD7800/7801 Functional Differences

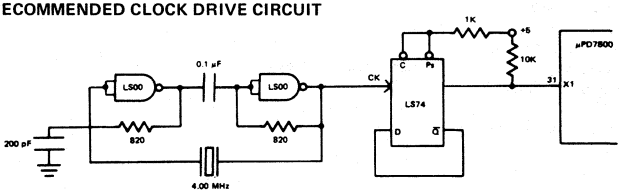
1. The functionality of μPD7801 Port E is somewhat different on the μPD7800. Because the μPD7800 contains no program memory, the address bus is made accessible to address external program memory. Thus, lines normally used for Port E operation with the μPD7801 are used as the address bus on the μPD7800. AB_0-AB_{15} is active during memory access 0 through 4095.
2. Consequently Port E instructions (PEX, PEN, and PER) have different functionality.

   PEX Instruction – The contents of B and C register are output to the address bus. The value 01H is output to the data bus. STB becomes active.

   PEN Instruction – B and C register contents are output to the address bus. The value 02H is output to the data bus. STB becomes active.

   PER Instruction – The address bus goes to the high impedance state. The value 04H is output to the data bus. STB becomes active.
3. ON-CHIP CLOCK GENERATOR. The μPD7800 contains no internal clock generator. An external clock source is input to the X_1 input.
4. PIN 30. This pin functions as the X_2 crystal connection on the μPD7801. On the μPD7800, pin 30 functions as a strobe output (STB) and becomes active when a Port E instruction is executed. This control signal is useful in simulating μPD7801 Port E operation – indicating that a port E operation is being performed.
5. PIN 2. Functions as the Φ out clock output used for synchronizing system external memory and I/O devices, on the μPD7801. On the μPD7800, this pin is used to simulate external memory reference operation of the μPD7801. $\overline{EXT}$ is used to distinguish between internal and external memory references and goes low when location 4096 through 65407 are accessed.

RECOMMENDED CLOCK DRIVE CIRCUIT



HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH 4K ROM

PRODUCT DESCRIPTION

The NEC μPD7801 is an advanced 8-bit general purpose single-chip microcomputer fabricated with N-Channel Silicon Gate MOS technology.

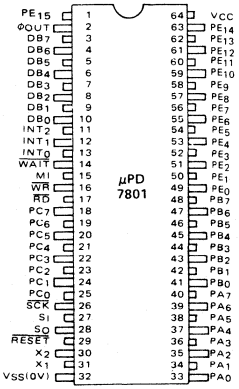
The NEC μPD7801 is intended to serve a broad spectrum of 8-bit designs ranging from enhanced single chip applications extending into the multi-chip microprocessor range. All the basic functional blocks – 4096 x 8 of ROM program memory, 128 x 8 of RAM data memory, 8-bit ALU, 48 I/O lines, Serial I/O port, 12-bit timer, and clock generator are provided on-chip to enhance standalone applications. Fully compatible with the industry standard 8080A bus structure, expanded system operation can be easily implemented using any of the 8080A/8085A peripherals and memory products. Total memory space can be increased to 64K bytes.

The powerful 140 instructions coupled with 4K bytes of ROM program memory and 128 bytes of RAM data memory greatly extends the range of single chip microcomputer applications. Five level vectored interrupt capability combined with a 2 microsecond cycle time enable the μPD7801 to compete with multi-chip microprocessor systems with the advantage that most of the support functions are on-chip.

FEATURES

- NMOS Silicon Gate Technology Requiring +5V Supply
- Complete Single-Chip Microcomputer with On-Chip ROM, RAM and I/O
  - 4K Bytes ROM
  - 128 Bytes RAM
  - 48 I/O Lines
- Internal 12-Bit Programmable Timer
- On-Chip 1 MHz Serial Port
- Five Level Vectored, Prioritized Interrupt Structure
  - Serial Port
  - Timer
  - 3 External Interrupts
- Bus Expansion Capabilities
  - Fully 8080A Bus Compatible
  - 60K Bytes External Memory Address Range
- On-Chip Clock Generator
- Wait State Capability
- Alternate Z80™ Type Register Set
- Powerful 140 Instructions
- 8 Address Modes; Including Auto-Increment/Decrement
- Multi-Level Stack Capabilities
- Fast 2 μs Cycle Time
- Bus Sharing Capabilities (DMA)

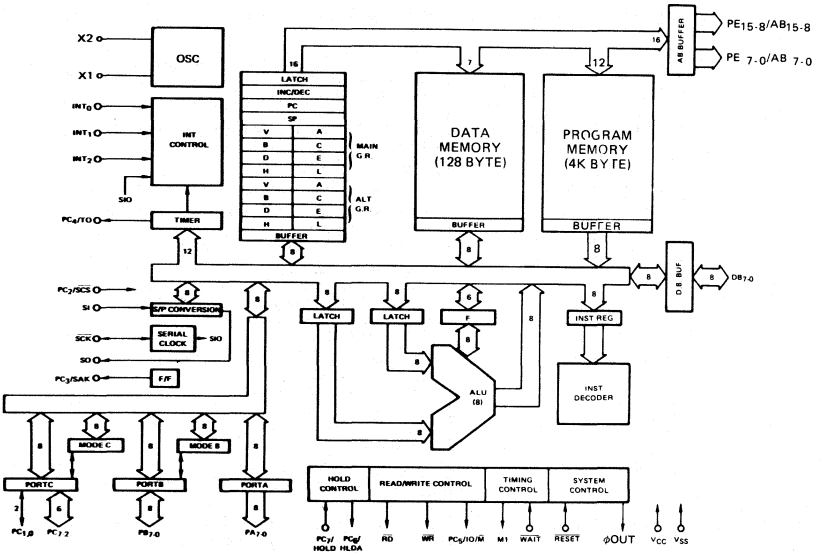
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	DESIGNATION	FUNCTION
1, 49-63	PE_0/AB_0-PE_{15}/AB_{15}	(Tri-State, Output) 16-bit address bus.
2	ϕOUT	(Output) ϕOUT provides a prescaled output clock for use with external I/O devices or memories. ϕOUT frequency is $f_{XTAL}/2$.
3-10	DB_0-DB_7	(Tri-State Input/Output, active high) 8-bit true bi-directional data bus used for external data exchanges with I/O and memory.
11	INT_0	(Input, active high) Level-sensitive interrupt input.
12	INT_1	(Input, active high) Rising-edge sensitive interrupt input. Interrupts are initiated on low-to-high transitions, providing interrupts are enabled.
13	INT_2	(Input) INT_2 is an edge sensitive interrupt input where the desired activation transition is programmable. By setting the ES bit in the Mask Register to a 1, INT_2 is rising edge sensitive. When ES is set to 0, INT_2 is falling edge sensitive.
14	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state TW and remains in that state as long as $\overline{WAIT}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-25	PC_0-PC_7	(Input/Output) 8-bit I/O configured as a nibble I/O port or as control lines.
26	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of SCK.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of SCK, MSB to LSB.
29	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD7801.
30	X_2	(Output) Oscillator output.
31	X_1	(Input) Clock Input.
33-40	PA_0-PA_7	(Output) 8-bit output port with latch capability.
41-48	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

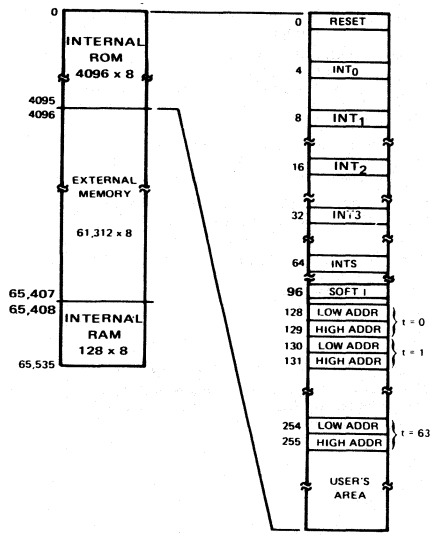
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Memory Map

The μPD7801 can directly address up to 64K bytes of memory. Except for the on-chip ROM (0-4096) and RAM (65.408-65.535), any memory location can be used as either ROM or RAM. The following memory map defines the 0-64K byte memory space for the μPD7801 showing that the Reset Start Address, Interrupt Start Address, Call Tables, etc., are located in the Internal ROM area.



HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH 6K ROM

PRODUCT DESCRIPTION

The NEC μPD7802 is an advanced 8-bit general purpose single-chip microcomputer fabricated with N-Channel Silicon Gate MOS technology.

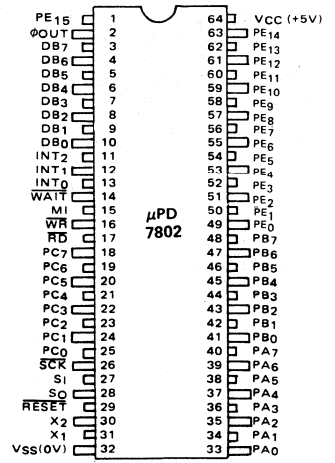
The NEC μPD7802 is intended to serve a broad spectrum of 8-bit designs ranging from enhanced single chip applications extending into the multi-chip microprocessor range. All the basic functional blocks – 6144 x 8 of ROM program memory, 64 x 8 of RAM data memory, 8-bit ALU, 48 I/O lines, Serial I/O port, 12-bit timer, and clock generator are provided on-chip to enhance standalone applications. Fully compatible with the industry standard 8080A bus structure, expanded system operation can be easily implemented using any of the 8080A/8085A peripherals and memory products. Total memory space can be increased to 64K bytes.

The powerful 140 instruction set coupled with 6K bytes of ROM program memory and 64 bytes of RAM data memory greatly extends the range of single chip microcomputer applications. Five level vectored interrupt capability combined with a 2 microsecond cycle time enable the μPD7802 to compete with multi-chip microprocessor systems with the advantage that most of the support functions are on-chip.

FEATURES

- NMOS Silicon Gate Technology Requiring +5V Supply
- Complete Single-Chip Microcomputer with On-Chip ROM, RAM and I/O
  - 6K Bytes ROM
  - 64Bytes RAM
  - 48 I/O Lines
- Internal 12-Bit Programmable Timer
- On-Chip 1 MHz Serial Port
- Five Level Vectored, Prioritized Interrupt Structure
  - Serial Port
  - Timer
  - 3 External Interrupts
- Bus Expansion Capabilities
  - Fully 8080A Bus Compatible
  - 58K Bytes External Memory Address Range
- On-Chip Clock Generator
- Wait State Capability
- Alternate Z80™ Type Register Set
- Powerful 140 Instructions
- 8 Address Modes; Including Auto-Increment/Decrement
- Multi-Level Stack Capabilities
- Fast 2 μs Cycle Time
- Bus Sharing Capabilities (DMA)

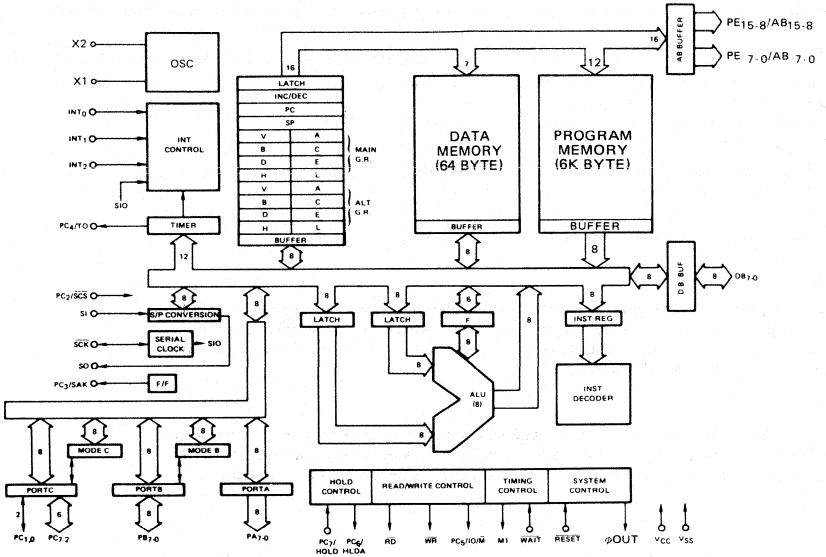
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	DESIGNATION	FUNCTION
1, 49-63	PE_0/AB_0-PE_{15}/AB_{15}	(Tri-State, Output) 16-bit address bus.
2	ϕOUT	(Output) ϕOUT provides a prescaled output clock for use with external I/O devices or memories. ϕOUT frequency is $f_{XTAL}/2$.
3-10	DB_0-DB_7	(Tri-State Input/Output, active high) 8-bit true bi-directional data bus used for external data exchanges with I/O and memory.
11	INT_0	(Input, active high) Level-sensitive interrupt input.
12	INT_1	(Input, active high) Rising-edge sensitive interrupt input. Interrupts are initiated on low-to-high transitions, providing interrupts are enabled.
13	INT_2	(Input) INT_2 is an edge sensitive interrupt input where the desired activation transition is programmable. By setting the ES bit in the Mask Register to a 1, INT_2 is rising edge sensitive. When ES is set to 0, INT_2 is falling edge sensitive.
14	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state T_W and remains in that state as long as $\overline{WAIT}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-25	PC_0-PC_7	(Input/Output) 8-bit I/O configured as a nibble I/O port or as control lines.
26	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of SCK.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of SCK, MSB to LSB.
29	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD7802.
30	X_2	(Output) Oscillator output.
31	X_1	(Input) Clock Input
33-40	PA_0-PA_7	(Output) 8-bit output port with latch capability.
41-48	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

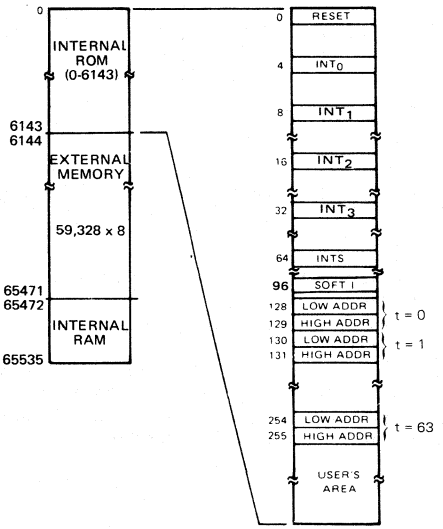
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Memory Map

The μPD7802 can directly address up to 64K bytes of memory. Except for the on-chip ROM (0-6143) and RAM(65.472-65.535), any memory location can be used as either ROM or RAM. The following memory map defines the 0-64K byte memory space for the μPD7802 showing that the Reset Start Address, Interrupt Start Address, Call Tables, etc., are located in the Internal ROM area.



FUNCTIONAL DESCRIPTION

I/O PORTS

PORT	FUNCTIONS
Port A	8-bit output port with latch
Port B	8-bit programmable Input/Output port w/latch
Port C	8-bit nibble I/O or Control port
Port E	16-bit Address/Output Port

Port A

Port A is an 8-bit latched output port. Data can be readily transferred between the accumulator and the output latch buffers. The contents of the output latches can be modified using Arithmetic and Logic instructions. Data remains latched at Port A unless acted on by another Port A instruction or a RESET is issued.

Port B

Port B is an 8-bit I/O port. Data is latched at Port B in both the Input or Output modes. Each bit of Port B can be independently set to either Input or Output modes. The Mode B register programs the individual lines of Port B to be either an Input (Mode $B_n = 1$) or an Output (Mode $B_n = 0$).

Port C

Port C is an 8-bit I/O port. The Mode C register is used to program the upper 6 bits of Port C to provide control functions or to set the I/O structure per the following table.

	MODE $C_n = 0$	MODE $C_n = 1$
PC_0	Output	Input
PC_1	Output	Input
PC_2	$\overline{SCS}$ Input	Input
PC_3	SAK Output	Output
PC_4	To Output	Output
PC_5	IO/$\overline{M}$ Output	Output
PC_6	HLDA Output	Output
PC_7	HOLD Input	Input

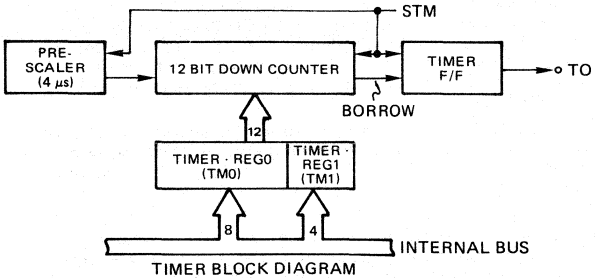
Port E

Port E is a 16-bit address bus/output port. It can be set to one of three operating modes using the PER, PEN, or PEX instructions.

- 16-Bit Address Bus – the PER instruction sets this mode for use with external I/O or memory expansion (up to 60K bytes, externally).
- 4-Bit Output Port/12 Bit Address Bus – the PEN instruction sets this mode which allows for memory expansion of an additional 4K bytes, externally, plus the transfer of 4-bit nibbles.
- 16-Bit Output Port – the PEX instructions sets Port E to a 16-bit output port. The contents of B and C registers appear on PE_{8-15} and PE_{0-7}, respectively.

FUNCTIONAL DESCRIPTION (CONT.)

TIMER OPERATION



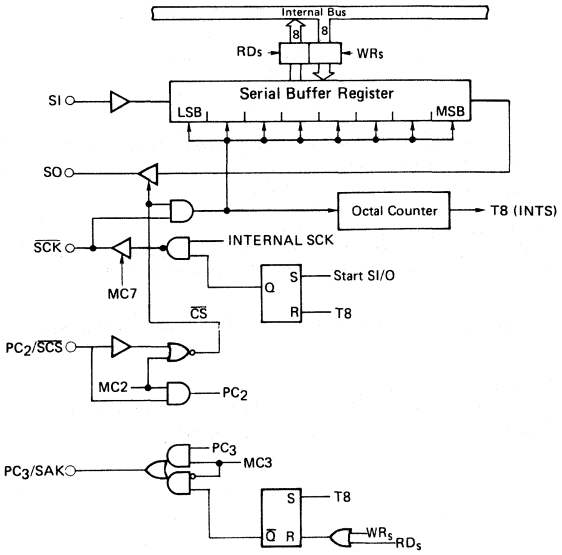
TIMER BLOCK DIAGRAM

A programmable 12-bit timer is provided on-chip for measuring time intervals, generating pulses, and general time-related control functions. It is capable of measuring time intervals from 4 μs to 16 ms in duration. The timer consists of a prescaler which decrements a 12-bit counter at a fixed 4 μs rate. Count pulses are loaded into the 12-bit down counter through timer register (TM0 and TM1). Count-down operation is initiated upon extension of the STM instruction when the contents of the down counter are fully decremented and a borrow operation occurs, an interval interrupt (INTT) is generated. At the same time, the contents of TM0 and TM1 are reloaded into the down-counter and countdown operation is resumed. Count operation may be restarted or initialized with the STM instruction. The duration of the timeout may be altered by loading new contents into the down counter.

The timer flip flop is set by the STM instruction and reset on a countdown operation. Its output (T0) is available externally and may be used in a single pulse mode or general external synchronization.

Timer interrupt (INTT) may be disabled through the interrupt.

SERIAL PORT OPERATION



SERIAL PORT BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION (CONT.)

The on-chip serial port provides basic synchronous serial communication functions allowing the NEC μPD7801/02 to serially interface with external devises.

Serial Transfers are synchronized with either the internal clock or an external clock input ($\overline{SCK}$). The transfer rate is fixed at 1 Mbit/second if the internal clock is used or is variable between DC and 1 Mbit/second when an external clock is used. The Clock Source Select is determined by the Mode C register. The serial clock (internal or external $\overline{SCK}$) is enabled when the Serial Chip Select Signal ($\overline{SCS}$) goes low. At this time receive and transmit operations through the Serial Input port (SI)/Serial Output port (SO) are enabled. Receive and transmit operations are performed MSB first.

Serial Acknowledge (SAK) goes high when data transfers between the accumulator and Serial Register is completed. SAK goes low when the buffer becomes full after the completion of serial data receive or transmit operations. While SAK is low, no further data can be received.

INTERRUPT STRUCTURE

The μPD7801/02 provides a maskable interrupt structure capable of handling vectored prioritized interrupts. Interrupts can be generated from six different sources; three external interrupts, two internal interrupts, and a non-maskable software interrupt. Each interrupt when activated branches to a designated memory vector location for that interrupt.

INT	VECTORED MEMORY LOCATION	PRIORITY	TYPE
INTT	8	3	Internal, Timer Overflow
INTS	64	6	Internal, Serial Buffer Full/Empty
INT0	4	2	Ext., level sensitive
INT1	16	4	Ext., Rising edge sensitive
INT2	32	5	Ext., Rising/Falling edge sensitive
SOFTI	96	1	Software Interrupt

$\overline{RESET}$ (Reset)

An active low-signal on this input for more than 4 μs forces the μPD7801/02 into a Reset condition. $\overline{RESET}$ affects the following internal functions:

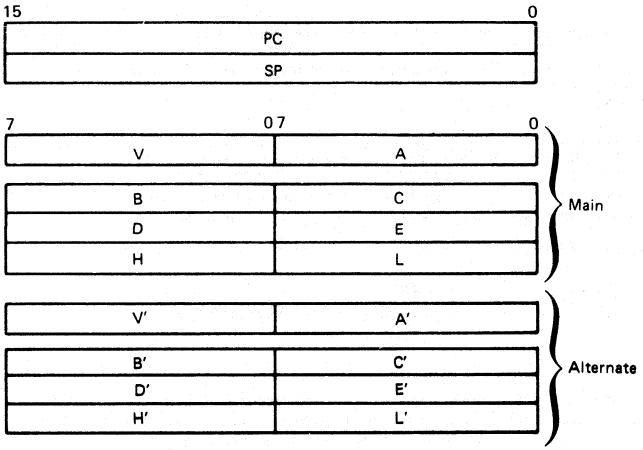
- The Interrupt Enable Flags are reset, and Interrupts are inhibited.
- The Interrupt Request Flag ist reset.
- The HALT flip flop is reset, and the Halt-state is released.
- The contents of the MODE B register are set to FF_H, and Port B becomes an input port.
- The contents of the MODE C register are set to FF_H. Port C becomes an I/O port and output lines go low.
- All Flags are reset to 0.
- The internal COUNT register for timer operation is set to FFF_H and the timer F/F is reset.
- The ACK F/F is set.
- The HLDA F/F is reset.
- The contents of the Program Counter are set to 0000_H.
- The Address Bus (PE_{0-15}), Data Bus (DB_{0-7}), $\overline{RD}$, and $\overline{WR}$ go to a high impedance state.

Once the $\overline{RESET}$ input goes high, the program is started at location 0000_H.

FUNCTIONAL DESCRIPTION (CONT.)

REGISTERS

The μPD7801/02 contains sixteen 8-bit registers and two 16-bit registers.



General Purpose Registers (B, C, D, E, H. L)

There are two sets of general purpose registers (Main: B, C, D, E, H, L: Alternate: B', C', D', E' H', L'). They can function as auxiliary registers to the accumulator or in pairs as data pointers (BC, DE, HL, B'C', D'E', H'L'). Auto Increment and Decrement adressing mode capabilities extend the uses for the DE, HL, D'E', and H'L' register-pairs. The contents of the BC, DE, and HL register-pairs can be exchanged with their Alternate Register counterparts using the EXX instruction.

Vector Register (V)

When defining a scratch pad area in the memory space, the upper 8-bit memory address is defined in the V-register and the lower 8-bits is defined by the immediate data of an instruction. Also the scratch pad indicated by the V-Register can be used as 256 x 8-bit working registers for storing software flags, parameters and counters immediately or directly.

Accumulator (A)

All data important data treatments on μPD7801/02 are done through the accumulator. The contents of the Accumulator and Vector Register can be exchanged with their Alternate Registers using the EX instruction.

Program Counter (PC)

The PC is a 16-bit register containing the address of the next instruction to be fetched. Under normal program flow, the PC is automatically incremented. However, in the case of a branch instruction, the PC contents comes from another register or an instruction's immediate data. A reset sets the PC to 0000_H.

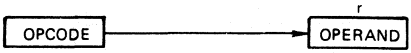
Stack Pointer (SP)

The stack pointer is a 16-bit register used to maintain the top of the stack area (last-in-first-out). The contents of the SP are decremented during a CALL or PUSH instruction or if an interrupt occurs. The SP is incremented during a RETURN or POP instruction.

ADDRESS MODES

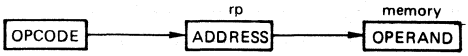
Register Addressing
Register Indirect Addressing
Auto-Increment Addressing
Auto-Decrement Addressing
Working Register Addressing
Direct Addressing
Immediate Addressing
Immediate Extended Addressing
Accumulator Indirect Adressing

Register Addressing



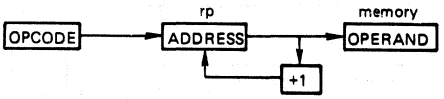
The instruction opcode specifies a register r which contains the operand.

Register Indirect Addressing



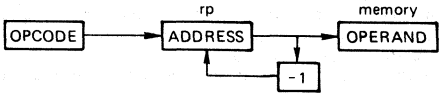
The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are ending this address mode.

Auto-Increment Addressing

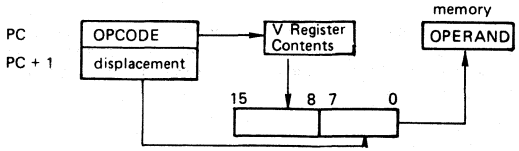


The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair is automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

Auto Decrement Addressing



Working Register Addressing

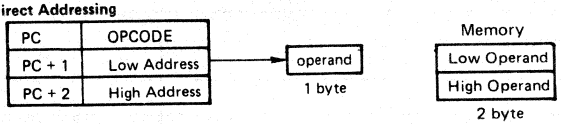


The contents of the register is linked with the byte following the opcode to form a memory address whose contents is the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only 1 additional byte is required for the address. The memory contents can be influenced directly or immediately. Mnemonics with a W suffix ending this address mode.

ADDRESS MODES (CONT.)

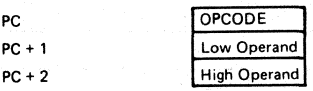
The two bytes following the opcode specify an address of a location containing the operand.

Direct Addressing



Immediate Addressing (8 bit)

Immediate Extended Addressing (16 bit)



Accumulator Indirect Adressing (Select Table)

C ← (PC + 2 + A)

B ← (PC + 2 + A + 1)

Operand Description

INSTRUCTION SET

OPERAND	DESCRIPTION
r	V, A, B, C, D, E, H, L
r1	B, C, D, E, H, L
r2	A, B, C
sr	PA PB PC MK MB MC TM0 TM1 S
sr1	PA PB PC MK S
sr2	PA PB PC MK
rp	SP, B, D, H
rp1	V, B, D, H
rpa	B, D, H, D+, H+, D−, H−
rpa1	B, D, H
wa	8 bit immediate data
word	16 bit immediate data
byte	8 bit immediate data
bit	3 bit immediate data
f	F0, F1, F2, FT, FS,

Notes:

1. When special register operands sr, sr1, sr2 are used; PA = Port A, PB = Port B, PC = Port C, MK = Mask Register, MB = Mode B Register, MC = Mode C Register, TM0 = Timer Register 0, TM1 = Timer Register 1, S = Serial Register.
2. When register pair operands rp, rp1 are used; SP = Stack Pointer, B = BC, D = DE, H = HL, V = VA.
3. Operands rpa, rpa1, wa are used in indirect addressing and auto-increment/auto-decrement addressing modes.
   B = (BC), D = (DE), H = (HL)
   D+ = (DE)+, H+ = (HL)+, D− = (DE)−, H− = (HL)−.
4. When the interrupt operand f is used; F0 = INTF0, F1 = INTF1, F2 = INTF2, FT = INTFT, FS = INTFS.

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
8-BIT DATA TRANSFER							
MOV	r1, A	1	4	r1 ← A			
MOV	A, r1	1	4	A ← r1			
MOV	sr, A	2	10	sr ← A			
MOV	A, sr1	2	10	A ← sr1			
MOV	r, word	4	17	r ← (word)			
MOV	word, r	4	17	(word) ← r			
MVI	r, byte	2	7	r ← byte			
MVIW	wa, byte	3	13	(V, wa) ← byte			
MVIX	rpa1, byte	2	10	(rpa1) ← byte			
STAW	wa	2	10	(V, wa) ← A			
LDAW	wa	2	10	A ← (V, wa)			
STAX	rpa	1	7	(rpa) ← A			
LDAX	rpa	1	7	A ← (rpa)			
EXX		1	4	Exchange register sets			
EX		1	4	V, A ↔ V', A'			
BLOCK		1	13 (C+1)	(DE) ← (HL), C ← C − 1 DE ← DE + 1 HL ←HL + 1			
16-BIT DATA TRANSFER							
SBCD	word	4	20	(word) ← C, (word + 1) ← B			
SDED	word	4	20	(word) ← E, (word + 1) ← D			
SHLD	word	4	20	(word) ← L, (word + 1) ← H			
SSPD	word	4	20	(word) ← SP_L, (word + 1) ← SP_H			
LBCD	word	4	20	C ← (word), B ← (word + 1)			
LDED	word	4	20	E ← (word), D ← (word + 1)			
LHLD	word	4	20	L ← (word), H ← (word + 1)			
LSPD	word	4	20	SP_L ← (word), SP_H ← (word + 1)			
PUSH	rp1	2	17	(SP − 1) ← $rp1_H$, (SP − 2) ← $rp1_L$			
POP	rp1	2	15	$rp1_L$ ← (SP) $rp1_H$ ← (SP + 1), SP ← SP + 2			
LXI	rp, word	3	10	rp ← word			
TABLE		1	19	C ← (PC + 2 + A) B ← (PC + 2 + A + 1)			

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
ARITHMETIC							
ADD	A, r	2	8	A ← A + r		↕	↕
ADD	r, A	2	8	r ← r + A		↕	↕
ADDX	rpa	2	11	A ← A + (rpa)		↕	↕
ADC	A, r	2	8	A ← A + r + CY		↕	↕
ADC	r, A	2	8	r ← r + A + CY		↕	↕
ADCX	rpa	2	11	A ← A + (rpa) + CY		↕	↕
SUB	A, r	2	8	A ← A − r		↕	↕
SUB	r, A	2	8	r ← r − A		↕	↕
SUBX	rpa	2	11	A ← A − (rpa)		↕	↕
SBB	A, r	2	8	A ← A − r − CY		↕	↕
SBB	r, A	2	8	r ← r − A − CY		↕	↕
SBBX	rpa	2	11	A ← A − (rpa) − CY		↕	↕
ADDNC	A, r	2	8	A ← A + r	No Carry	↕	↕
ADDNC	r, A	2	8	r ← r + A	No Carry	↕	↕
ADDNCX	rpa	2	11	A ← A + (rpa)	No Carry	↕	↕
SUBNB	A, r	2	8	A ← A − r	No Borrow	↕	↕
SUBNB	r, A	2	8	r ← r − A	No Borrow	↕	↕
SUBNBX	rpa	2	11	A ← A − (rpa)	No Borrow	↕	↕
LOGICAL							
ANA	A, r	2	8	A ← A ∧ r			↕
ANA	r, A	2	8	r ← r ∧ A			↕
ANAX	rpa	2	11	A ← A ∧ (rpa)			↕
ORA	A, r	2	8	A ← A ∨ r			↕
ORA	r, A	2	8	r ← r ∨ A			↕
ORAX	rpa	2	11	A ← A ∨ (rpa)			↕
XRA	A, r	2	8	A ← A ∨̄ r			↕
XRA	r, A	2	8	A ← r ∨̄ A			↕
XRAX	rpa	2	11	A ← A ∨̄ (rpa)			↕
GTA	A, r	2	8	A − r − 1	No Borrow	↕	↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
LOGICAL (CONT.)							
GTAX	rpa	2	11	A - (rpa) - 1	No Borrow	↕	↕
LTA	A, r	2	8	A - r	Borrow	↕	↕
LTA	r, A	2	8	r - A	Borrow	↕	↕
LTAX	rpa	2	11	A - (rpa)	Borrow	↕	↕
ONA	A, r	2	8	A ∧ r	No Zero		↕
ONAX	rpa	2	11	A ∧ (rpa)	No Zero		↕
OFFA	A, r	2	8	A ∧ r	Zero		↕
OFFAX	rpa	2	11	A ∧ (rpa)	Zero		↕
NEA	A, r	2	8	A - r	No Zero	↕	↕
NEA	r, A	2	8	r - A	No Zero	↕	↕
NEAX	rpa	2	11	A - (rpa)	No Zero	↕	↕
EQA	A, r	2	8	A - r	Zero	↕	↕
EQA	r, A	2	8	r - A	Zero	↕	↕
EQAX	rpa	2	11	A - (rpa)	Zero	↕	↕
IMMEDIATE DATA TRANSFER (ACCUMULATOR)							
XRI	A, byte	2	7	A ← A ∨ byte			↕
ADINC	A, byte	2	7	A ← A + byte	No Carry	↕	↕
SUINB	A, byte	2	7	A ← A - byte	No Borrow	↕	↕
ADI	A, byte	2	7	A ← A + byte		↕	↕
ACI	A, byte	2	7	A ← A + byte + CY		↕	↕
SUI	A, byte	2	7	A ← A - byte		↕	↕
SBI	A, byte	2	7	A ← A - byte - CY		↕	↕
ANI	A, byte	2	7	A ← A ∧ byte			↕
ORI	A, byte	2	7	A ← A ∨ byte			↕
GTI	A, byte	2	7	A - byte - 1	No Borrow	↕	↕
LTI	A, byte	2	7	A - byte	Borrow	↕	↕
ONI	A, byte	2	7	A ∧ byte	No Zero		↕
OFFI	A, byte	2	7	A ∧ byte	Zero		↕
NEI	A, byte	2	7	A - byte	No Zero	↕	↕
EQI	A, byte	2	7	A - byte	Zero	↕	↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
IMMEDIATE DATA TRANSFER							
XRI	r, byte	3	11	r ← r ⊻ byte			↕
ADINC	r, byte	3	11	r ← r + byte	No Carry	↕	↕
SUINB	r, byte	3	11	r ← r − byte	No Borrow	↕	↕
ADI	r, byte	3	11	r ← r + byte		↕	↕
ACI	r, byte	3	11	r ← r + byte + CY		↕	↕
SUI	r, byte	3	11	r ← r − byte		↕	↕
SBI	r, byte	3	11	r ← r − byte − CY		↕	↕
ANI	r, byte	3	11	r ← r ∧ byte		↕	↕
ORI	r, byte	3	11	r ← r ∨ byte			↕
GTI	r, byte	3	11	r − byte − 1	No Borrow	↕	↕
LTI	r, byte	3	11	r − byte	Borrow	↕	↕
ONI	r, byte	3	11	r ∧ byte	No Zero		↕
OFFI	r, byte	3	11	r ∧ byte	Zero		↕
NEI	r, byte	3	11	r ≠ byte	No Zero	↕	↕
EQI	r, byte	3	11	r − byte	Zero	↕	↕
IMMEDIATE DATA TRANSFER (SPECIAL REGISTER)							
XRI	sr2, byte	3	17	sr2 ← sr2 ⊻ byte			↕
ADINC	sr2, byte	3	17	sr2 ← sr2 + byte	No Carry	↕	↕
SUINB	sr2, byte	3	17	sr2 ← sr2 − byte	No Borrow	↕	↕
ADI	sr2, byte	3	17	sr2 ← sr2 + byte		↕	↕
ACI	sr2, byte	3	17	sr2 ← sr2 + byte + CY		↕	↕
SUI	sr2, byte	3	17	sr2 ← sr2 − byte		↕	↕
SBI	sr2, byte	3	17	sr2 ← sr2 − byte − CY		↕	↕
ANI	sr2, byte	3	17	sr2 ← sr2 ∧ byte			↕
ORI	sr2, byte	3	17	sr2 ← sr2 ∨ byte			↕
GTI	sr2, byte	3	14	sr2 − byte − 1	No Borrow	↕	↕
LTI	sr2, byte	3	14	sr2 − byte	Borrow	↕	↕
ONI	sr2, byte	3	14	sr2 ∧ byte	No Zero		↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
IMMEDIATE DATA TRANSFER (SPECIAL REGISTER) (CONT.)							
OFFI	sr2, byte	3	14	sr2 ∧ byte	Zero		↕
NEI	sr2, byte	3	14	sr2 - byte	No Zero	↕	↕
EQI	sr2, byte	3	14	sr2 - byte	Zero	↕	↕
WORKING REGISTER							
XRAW	wa	3	14	A ← A ∀ (V, wa)			↕
ADDNCW	wa	3	14	A ← A + (V, wa)	No Carry	↕	↕
SUBNBW	wa	3	14	A ← A - (V, wa)	No Borrow	↕	↕
ADDW	wa	3	14	A ← A + (V, wa)		↕	↕
ADCW	wa	3	14	A ← A + (V, wa) + CY		↕	↕
SUBW	wa	3	14	A ← A - (V, wa)		↕	↕
SBBW	wa	3	14	A ← A - (V, wa) - CW		↕	↕
ANAW	wa	3	14	A ← A ∧ (V, wa)			↕
ORAW	wa	3	14	A ← A ∨ (V, wa)			↕
GTAW	wa	3	14	A ← (V, wa) - 1	No Borrow	↕	↕
LTAW	wa	3	14	A - (V, wa)	Borrow	↕	↕
ONAW	wa	3	14	A ∧ (V, wa)	No Zero		↕
OFFAW	wa	3	14	A ∧ (V, wa)	Zero		↕
NEAW	wa	3	14	A - (V, wa)	No Zero	↕	↕
EQAW	wa	3	14	A - (V, wa)	Zero	↕	↕
ANIW	wa, byte	3	16	(V, wa) ← (V, wa) ∧ byte			↕
ORIW	wa, byte	3	16	(V, wa) ← (V, wa) ∨ byte			↕
GTIW	wa, byte	3	13	(V, wa) - byte - 1	No Borrow	↕	↕
LTIW	wa, byte	3	13	(V, wa) - byte	Borrow	↕	↕
ONIW	wa, byte	3	13	(V, wa) ∧ byte	No Zero		↕
OFFIW	wa, byte	3	13	(V, wa) ∧ byte	Zero		↕
NEIW	wa, byte	3	13	(V, wa) - byte	No Zero	↕	↕
EQIW	wa, byte	3	13	(V, wa) - byte	Zero	↕	↕
INCREMENT/DECREMENT							
INR	r2	1	4	r2 ← r2 + 1	Carry		↕
INRW	wa	2	13	(V, wa) ← (V, wa) + 1	Carry		↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
INCREMENT/DECREMENT (CONT.)							
DCR	r2	1	4	r2 ← r2 - 1	Borrow		↕
DCRW	wa	2	13	(V, wa) ← (V, wa) - 1	Borrow		↕
INX	rp	1	7	rp ← rp + 1			
DCX	rp	1	7	rp ← rp - 1			
DAA		1	4	Decimal Adjust Accumulator		↕	↕
STC		2	8	CY ← 1		1	
CLC		2	8	CY ← 0		0	
ROTATE AND SHIFT							
RLD		2	17	Rotate Left Digit			
RRD		2	17	Rotate Right Digit			
RAL		2	8	Am + 1 ← Am, A_0 ← CY, CY ← A_7		↕	
RCL		2	8	Cm + 1 ← Cm, C_0 ← CY, CY ← C_7		↕	
RAR		2	8	Am - 1 ← Am, A_7 ← CY, CY ← A_0		↕	
RCR		2	8	Cm - 1 ← Cm, C_7 ← CY, CY ← C_0		↕	
SHAL		2	8	Am + 1 ← Am, A_0 ← 0, CY ← A_7		↕	
SHCL		2	8	Cm + 1 ← CM, C_0 ← 0, CY ← C_7		↕	
SHAR		2	8	Am - 1 ← Am, A_7 ← 0, CY ← A_0		↕	
SHCR		2	8	Cm - 1 ← Cm, C_7 ← 0, CY ← C_0		↕	
JUMP							
JMP	word	3	10	PC ← word			
JB		1	4	PC_H ← B, PC_L ← C			
JR	word	1	13	PC ← PC + 1 + jdisp1			
JRE	word	2	13	PC ← PC + 2 + jdisp			
CALL							
CALL	word	3	16	(SP - 1) ← $(PC - 3)_H$, (SP - 2) ← $(PC - 3)_L$, PC ← word			
CALB		1	13	(SP -,1) ← $(PC - 1)_H$, (SP - 2) ← $(PC - 1)_L$, PC_H ← B, PC_L ← C			
CALF	word	2	16	$(SP-1)\leftarrow(PC-2)_H$, $(SP-2)\leftarrow(PC-2)_L$ PC15 ~ 11 ← 00001, PC10 ~ 0 ← fa			
CALT	word	1	19	$(SP-1)\leftarrow(PC-1)_H$, $(SP-2)\leftarrow(PC-1)_L$ $PC_L\leftarrow(128-2ta)$, $PC_H\leftarrow(129+2ta)$			
SOFTI		1	19	(SP - 1) ← PSW, SP - 2, (SP - 3) ← PC PC ← 0060_H, SIRQ ← 1			

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
RETURN							
RET		1	11	$PC_L \leftarrow (SP), PC_H \leftarrow (SP+1)$ $SP \leftarrow SP-2$			
RETS		1	11+a	$PC_L \leftarrow (SP), PC_H \leftarrow (SP+1)$, $SP \leftarrow SP+2, PC \leftarrow PC+n$			
RETI		1	15	$PC_L \leftarrow (SP), PC_H \leftarrow (SP+1)$ $PSW \leftarrow (SP+2), SP \leftarrow SP+3, SIRQ \leftarrow 0$			
SKIP							
BIT	bit, wa	2	10	Bit test	$(V, wa)_{bit} = 1$		
SKC		2	8	Skip if Carry	CY = 1		
SKNC		2	8	Skip if No Carry	CY = 0		
SKZ		2	8	Skip if Zero	Z = 1		
SKNZ		2	8	Skip if No Zero	Z = 0		
SKIT	f	2	8	Skip if INT X = 1, then reset INT X	f = 1		
SKNIT	f	2	8	Skip if No INT X otherwise reset INT X	f = 0		
CPU CONTROL							
NOP		1	4	No Operation			
EI		2	8	Enable Interrupt			
DI		2	8	Disable Interrupt			
HLT		1	6	Halt			
SERIAL PORT CONTROL							
SIO		1	4	Start (Trigger) Serial I/O			
STM		1	4	Start Timer			
INPUT/OUTPUT							
IN	byte	2	10	$AB_{15-8} \leftarrow B, AB_{7-0} \leftarrow byte$ $A \leftarrow DB_{7-0}$			
OUT	byte	2	10	$AB_{15-8} \leftarrow B, AB_{7-0} \leftarrow byte$ $DB_{7-0} \leftarrow A$			
PEX		2	11	$PE_{15-8} \leftarrow B, PE_{7-0} \leftarrow C$			
PEN		2	11	$PE_{15-12} \leftarrow B_{7-4}$			
PER		2	11	Port E AB Mode			

Program Status Word (PSW) Operation

OPERATION						D6	D5	D4	D3	D2	D0
REG, MEMORY			IMMEDIATE		SKIP	Z	SK	HC	L1	L0	CY
ADD ADC SUB SBB	ADDW ADCW SUBW SBBW	ADDX ADCX SUBX SBBX	ADI ACI SUI SBI			↕	0	↕	0	0	↕
ANA ORA XRA	ANAW ORAW XRAW	ANAX ORAX XRAX	ANI ORI XRI	ANIW ORIW		↕	0	•	0	0	•
ADDNC SUBNB GTA LTA	ADDNCW SUBNBW GTAW LTAW	ADDNCX SUBNBX GTAX LTAX	ADINC SUINB GTI LTI	 GTIW LTIW		↕	↕	↕	0	0	↕
ONA OFFA	ONAW OFFAW	ONAX OFFAX	ONI OFFI	ONIW OFFIW		↕	↕	•	0	0	•
NEA EQA	NEAW EQAW	NEAX EQAX	NEI EQI	NEIW EQIW		↕	↕	↕	0	0	↕
INR DCR	INRW DCRW					↕	↕	↕	0	0	•
DAA						↕	0	↕	0	0	↕
RAL, RAR, RCL, RCR SHAL, SHAR, SHCL, SHCR						•	0	•	0	0	↕
RLD, RRD						•	0	•	0	0	•
STC						•	0	•	0	0	1
CLC						•	0	•	0	0	0
			MVI A, byte			•	0	•	1	0	•
			MVI L, byte LXI H, word			•	0	•	0	1	•
					BIT SKC SKNC SKZ SKNZ SKIT SKNIT	•	↕	•	0	0	•
					RETS	•	1	•	0	0	•
All other instructions						•	0	•	0	0	•

↕ Flag affected according to result of operation
1 Flag set
0 Flag reset
• Flag not affected

ELECTRICAL SPECIFICATIONS AND PACKAGE OUTLINES FOR

μPD7800/μPD7801/μPD7802

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C

Storage Temperature . . . . . −65°C to +125°C

Voltage On Any Pin . . . . . −0.3V to +7.0V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10 ~ +70°C, V_{CC} = +5.0V ± 10 %

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	0		0.8	V	
Input High Voltage	V_{IH1}	2.0		V_{CC}	V	Except $\overline{SCK}$, X1
	V_{IH2}	3.8		V_{CC}	V	$\overline{SCK}$, X1
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −100 μA
	V_{OH2}	2.0			V	I_{OH} = −500 μA
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_{IN} = 0V
High Level Input Leakage Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = 0.45V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Power Supply Current	I_{CC}		110	200	mA	

CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_I			10	pF	fc = 1 MHz All pins not under test at 0V
Output Capacitance	C_O			20	pF	
Input/Output Capacitance	C_{IO}			20	pF	

AC CHARACTERISTICS

CLOCK TIMING

T_a = −10 to +70°C, V_{CC} = +5.0V ± 10 %, $f_{osz\ max}$ = 2 MHz, not devided internally

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
X_{OUT} Cycle Time	t_{CYX}	454	2000	ns	t_{CYX}
X_{OUT} Low Level Width	t_{XXL}	212		ns	t_{XXL}
X_{OUT} High Level Width	t_{XXH}	212		ns	t_{XXH}

READ/WRITE OPERATION

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
$\overline{RD}$ L.E. → X_{OUT} L.E.	t_{RX}	20		ns	
Address ($PE_{0\text{-}15}$) → Data Input	t_{AD1}		550 + 500 x N	ns	
$\overline{RD}$ T.E. → Address	t_{RA}	200(T3); 700(T4)		ns	
$\overline{RD}$ L.E. → Data Input	t_{RD}		350 + 500 x N	ns	
$\overline{RD}$ T.E. → Data Hold Time	t_{RDH}	0		ns	
$\overline{RD}$ Low Level Width	t_{RR}	850 + 500 x N		ns	
$\overline{RD}$ L.E. → $\overline{WAIT}$ L.E.	t_{RWT}		450	ns	
Address ($PE_{0\text{-}15}$) → $\overline{WAIT}$ L.E.	t_{AWT1}		650	ns	
$\overline{WAIT}$ Set Up Time (Referenced from X_{OUT} L.E.)	t_{WTS}	180		ns	
$\overline{WAIT}$ Hold Time (Referenced from X_{OUT} L.E.)	t_{WTH}	0		ns	
M1 → $\overline{RD}$ L.E.	t_{MR}	200		ns	t_{CYX} = 500 ns
$\overline{RD}$ T.E. → M1	t_{RM}	200		ns	
IO/$\overline{M}$ → $\overline{RD}$ L.E.	t_{IR}	200		ns	
$\overline{RD}$ T.E. → IO/$\overline{M}$	t_{RI}	200		ns	
X_{OUT} L.E. → $\overline{WR}$ L.E.	t_{XW}		270	ns	
Address ($PE_{0\text{-}15}$) → X_{OUT} T.E.	t_{AX}		300	ns	
Address ($PE_{0\text{-}15}$) → Data Output	t_{AD2}	450		ns	
Data Output → $\overline{WR}$ T.E.	t_{DW}	600 + 500 x N		ns	
$\overline{WR}$ T.E. → Data Stabilization Time	t_{WD}	150		ns	
Address ($PE_{0\text{-}15}$) → $\overline{WR}$ L.E.	t_{AW}	400		ns	
$\overline{WR}$ T.E. → Address Stabilization Time	t_{WA}	200		ns	
$\overline{WR}$ Low Level Width	t_{WW}	600 + 500 x N		ns	
IO/$\overline{M}$ → $\overline{WR}$ L.E.	t_{IW}	500		ns	
$\overline{WR}$ T.E. → IO/$\overline{M}$	t_{WI}	250		ns	

AC CHARACTERISTICS (CONT.)

SERIAL I/O OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
$\overline{SCK}$ Cycle Time	t_{CYK}	800		ns	$\overline{SCK}$ Input
		900	4000	ns	$\overline{SCK}$ Output
$\overline{SCK}$ Low Level Width	t_{KKL}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
$\overline{SCK}$ High Level Width	t_{KKH}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
SI Set-Up Time (referenced from $\overline{SCK}$ T.E.)	t_{SIS}	140		ns	
SI Hold Time (referenced from $\overline{SCK}$ T.E.)	t_{SIH}	260		ns	
$\overline{SCK}$ L.E. → SO Delay Time	t_{KO}		180	ns	
$\overline{SCS}$ High → $\overline{SCK}$ L.E.	t_{CSK}	100		ns	
$\overline{SCK}$ T.E. → $\overline{SCS}$ Low	t_{KCS}	100		ns	
$\overline{SCK}$ T.E. → SAK Low	t_{KSA}		260	ns	

PEN, PEX, PER OPERATION

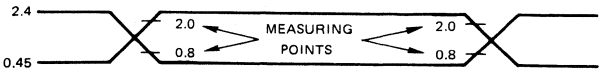
PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
X_1 L.E. → $\overline{EXT}$	t_{XE}		250	ns	t_{CYX} = 500 ns
Address ($AB_{0\text{-}15}$) → STB L.E.	t_{AST}	200			
Data ($DB_{0\text{-}7}$) → STB L.E.	t_{DST}	200			
STB Hold Time	t_{STST}	300			
STB → Data	t_{STD}	400			

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from X_{OUT} L.E.)	t_{HDS_1}	100		ns	
	t_{HDS_2}	100		ns	
HOLD Hold Time (referenced from ϕ_{OUT} L.E.)	t_{HDH}	100		ns	
X_{OUT} L.E. → HLDA	t_{XHA}		100	ns	
HLDA High → Bus Floating (High Z State)	t_{HABF}	−150	150	ns	
HLDA Low → Bus Enable	t_{HABE}		350	ns	

Notes:

① AC Signal waveform (unless otherwise specified)



② Output Timing is measured with 1 TTL + 200 pF measuring points are V_{OH} = 2.0V
V_{OL} = 0.8V

③ L.E. = Leading Edge, T.E. = Trailing Edge

AC CHARACTERISTICS (CONT.)

t_{CYX} DEPENDENT AC PARAMETERS

PARAMETER	EQUATION	MIN/MAX	UNIT
t_{RX}	(1/25) T	MIN	ns
t_{AD_1}	(3/2 + N) T - 200	MAX	ns
t_{RA} (T_3)	(1/2) T - 50	MIN	ns
t_{RA} (T_4)	(3/2) T - 50	MIN	ns
t_{RD}	(1 + N) T - 150	MAX	ns
t_{RR}	(2 + N) T - 150	MIN	ns
t_{RWT}	(3/2) T - 300	MAX	ns
t_{AWT_1}	(2) T - 350	MAX	ns
t_{MR}	(1/2) T - 50	MIN	ns
t_{RM}	(1/2) T - 50	MIN	ns
t_{IR}	(1/2) T - 50	MIN	ns
t_{RI}	(1/2) T - 50	MIN	ns
t_{XW}	(27/50) T	MAX	ns
t_{AD_2}	T - 50	MIN	ns
t_{DW}	(3/2 + N) T - 150	MIN	ns
t_{WD}	(1/2) T - 100	MIN	ns
t_{AW}	T - 100	MIN	ns
t_{WA}	(1/2) T - 50	MIN	ns
t_{WW}	(3/2 + N) T - 150	MIN	ns
t_{IW}	T	MIN	ns
t_{WI}	(1/2) T	MIN	ns
t_{HABE}	(1/2) T - 150	MAX	ns
t_{AST}	(2/5) T	MIN	ns
t_{DST}	(2/5) T	MIN	ns
t_{STST}	(3/5) T	MIN	ns
t_{STD}	(4/5) T	MIN	ns

Notes: ① N = Number of Wait States

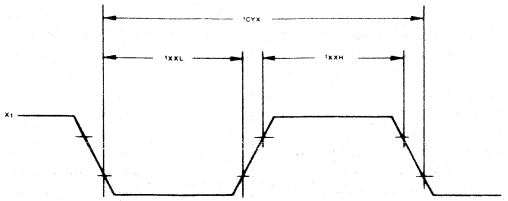
② T = t_{CYX}

③ Only above parameters are t_{CYX} dependent

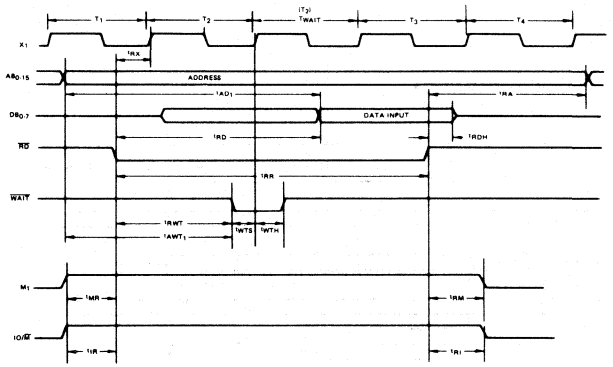
④ When a crystal frequency other than 4 MHz is used (t_{CYX} = 500 ns) the above equations can be used to calculate AC parameter values.

TIMING WAVEFORMS

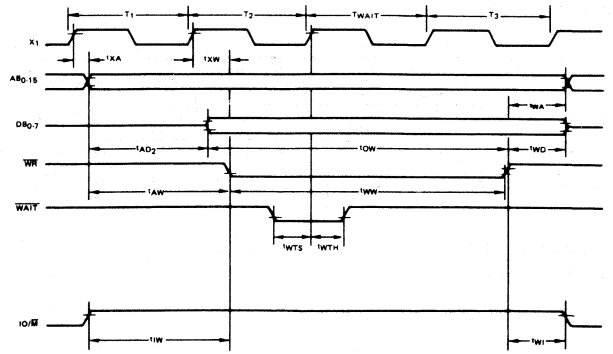
CLOCK TIMING



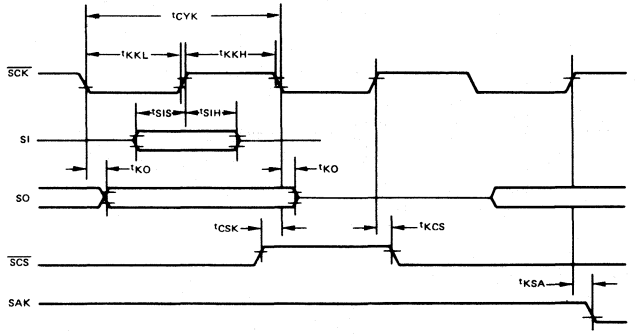
READ OPERATION



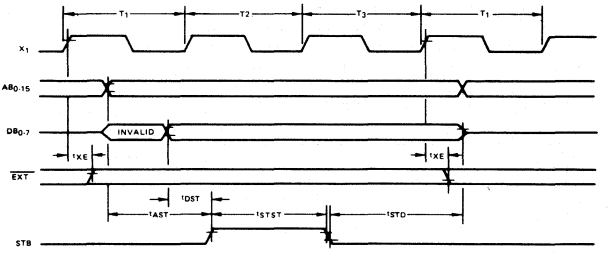
WRITE OPERATION



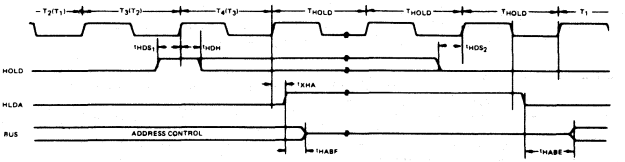
SERIAL I/O OPERATION



PEN, PEX, PER OPERATION



HOLD OPERATION



PACKAGE OUTLINES

Plastic Quil, μPD7800G

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Voltage On Any Pin . . . . . −0.3V to +7.0V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC CHARACTERISTICS

$T_a = -10$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	0		0.8	V	
Input High Voltage	V_{IH1}	2.0		V_{CC}	V	Except $\overline{SCK}$, X1
	V_{IH2}	3.8		V_{CC}	V	$\overline{SCK}$, X1
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 2.0$ mA
Output High Voltage	V_{OH1}	2.4			V	$I_{OH} = -100\ \mu A$
	V_{OH2}	2.0			V	$I_{OH} = -500\ \mu A$
Low Level Input Leakage Current	I_{LIL}			-10	μA	$V_{IN} = 0V$
High Level Input Leakage Current	I_{LIH}			10	μA	$V_{IN} = V_{CC}$
Low Level Output Leakage Current	I_{LOL}			-10	μA	$V_{OUT} = 0.45V$
High Level Output Leakage Current	I_{LOH}			10	μA	$V_{OUT} = V_{CC}$
V_{CC} Power Supply Current	I_{CC}		110	200	mA	

CAPACITANCE

$T_a = 25°C$, $V_{CC} = GND = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_I			10	pF	fc = 1 MHz All pins not under test at 0V
Output Capacitance	C_O			20	pF	
Input/Output Capacitance	C_{IO}			20	pF	

CLOCK TIMING

−10 to +70°C, V_{CC} = +5.0V ± 10 %, $f_{osz\ max}$ = 4 MHz, internally devided (1:2)

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
X1 Input Cycle Time	t_{CYX}	227	1000	ns	
X1 Input Low Level Width	t_{XXL}	106		ns	
X1 Input High Level Width	t_{XXH}	106		ns	
ϕ_{OUT} Cycle Time	$t_{CY\phi}$	454	2000	ns	
ϕ_{OUT} Low Level Width	$t_{\phi\phi L}$	150		ns	
ϕ_{OUT} High Level Width	$t_{\phi\phi H}$	150		ns	
ϕ_{OUT} Rise/Fall Time	$t_{r,tf}$		40	ns	

READ/WRITE OPERATION

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
$\overline{RD}$ L.E. → ϕ_{OUT} L.E.	$t_{R\phi}$	100		ns	
Address (PE_{0-15}) → Data Input	t_{AD1}		550 + 500 x N	ns	
$\overline{RD}$ T.E. → Address	t_{RA}	200(T3); 700(T4)		ns	
$\overline{RD}$ L.E. → Data Input	t_{RD}		350 + 500 x N	ns	
$\overline{RD}$ T.E. → Data Hold Time	t_{RDH}	0		ns	
$\overline{RD}$ Low Level Width	t_{RR}	850 + 500 x N		ns	
$\overline{RD}$ L.E. → $\overline{WAIT}$ L.E.	t_{RWT}		450	ns	
Address (PE_{0-15}) → WAIT L.E.	t_{AWT1}		650	ns	
$\overline{WAIT}$ Set Up Time (Referenced from ϕ_{OUT} L.E.)	t_{WTS}	290		ns	
$\overline{WAIT}$ Hold Time (Referenced from ϕ_{OUT} L.E.)	t_{WTH}	0	120	ns	
M1 → $\overline{RD}$ L.E.	t_{MR}	200		ns	$t_{CY\phi}$ = 500 ns
$\overline{RD}$ T.E. → M1	t_{RM}	200		ns	
IO/$\overline{M}$ → $\overline{RD}$ L.E.	t_{IR}	200		ns	
$\overline{RD}$ T.E. → IO/$\overline{M}$	t_{RI}	200		ns	
ϕ_{OUT} L.E. → $\overline{WR}$ L.E.	$t_{\phi W}$	40	125	ns	
Address (PE_{0-15}) → ϕ_{OUT} T.E.	$t_{A\phi}$	100		ns	
Address (PE_{0-15}) → Data Output	t_{AD2}	450		ns	
Data Output → $\overline{WR}$ T.E.	t_{DW}	600 + 500 x N		ns	
$\overline{WR}$ T.E. → Data Stabilization Time	t_{WD}	150		ns	
Address (PE_{0-15}) → $\overline{WR}$ L.E.	t_{AW}	400		ns	
$\overline{WR}$ T.E. → Address Stabilization Time	t_{WA}	200		ns	
$\overline{WR}$ Low Level Width	t_{WW}	600 + 500 x N		ns	
IO/$\overline{M}$ → $\overline{WR}$ L.E.	t_{IW}	500		ns	
$\overline{WR}$ T.E. → IO/$\overline{M}$	t_{WI}	250		ns	

SERIAL I/O OPERATION

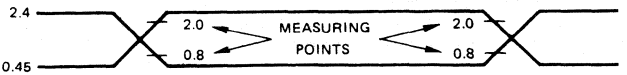
PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
$\overline{SCK}$ Cycle Time	t_{CYK}	800		ns	$\overline{SCK}$ Input
		900	4000	ns	$\overline{SCK}$ Output
$\overline{SCK}$ Low Level Width	t_{KKL}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
$\overline{SCK}$ High Level Width	t_{KKH}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
SI Set-Up Time (referenced from $\overline{SCK}$ T.E.)	t_{SIS}	80		ns	
SI Hold Time (referenced from $\overline{SCK}$ T.E.)	t_{SIH}	260		ns	
$\overline{SCK}$ L.E. → SO Delay Time	t_{KO}		180	ns	
$\overline{SCS}$ High → $\overline{SCK}$ L.E.	t_{CSK}	100		ns	
$\overline{SCK}$ T.E. → $\overline{SCS}$ Low	t_{KCS}	100		ns	
$\overline{SCK}$ T.E. → SAK Low	t_{KSA}		260	ns	

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from ϕ_{OUT} L.E.)	t_{HDS1}	200		ns	$t_{CY\phi}$ = 500 ns
	t_{HDS2}	200		ns	
HOLD Hold Time (referenced from ϕ_{OUT} L.E.)	t_{HDH}	0		ns	
ϕ_{OUT} L.E. → HLDA	$t_{\phi HA}$	−110	100	ns	
HLDA High → Bus Floating (High Z State)	t_{HABF}	−150	150	ns	
HLDA Low → Bus Enable	t_{HABE}		350	ns	

Notes:

① AC Signal waveform (unless otherwise specified)



② Output Timing is measured with 1 TTL + 200 pF measuring points are V_{OH} = 2.0V
V_{OL} = 0.8V

③ L.E. = Leading Edge, T.E. = Trailing Edge

AC CHARACTERISTICS (CONT.)

$t_{CY\phi}$ DEPENDENT AC PARAMETERS

PARAMETER	EQUATION	MIN/MAX	UNIT
$t_{R\phi}$	(1/5) T	MIN	ns
t_{AD_1}	(3/2 + N) T - 200	MAX	ns
t_{RA} (T_3)	(1/2) T - 50	MIN	ns
t_{RA} (T_4)	(3/2) T - 50	MIN	ns
t_{RD}	(1 + N) T - 150	MAX	ns
t_{RR}	(2 + N) T - 150	MIN	ns
t_{RWT}	(3/2) T - 300	MAX	ns
t_{AWT_1}	(2) T - 350	MAX	ns
t_{MR}	(1/2) T - 50	MIN	ns
t_{RM}	(1/2) T - 50	MIN	ns
t_{IR}	(1/2) T - 50	MIN	ns
t_{RI}	(1/2) T - 50	MIN	ns
$t_{\phi W}$	(1/4) T	MAX	ns
$t_{A\phi}$	(1/5) T	MIN	ns
t_{AD_2}	T - 50	MIN	ns
t_{DW}	(3/2 + N) T - 150	MIN	ns
t_{WD}	(1/2) T - 100	MIN	ns
t_{AW}	T - 100	MIN	ns
t_{WA}	(1/2) T - 50	MIN	ns
t_{WW}	(3/2 + N) T - 150	MIN	ns
t_{IW}	T	MIN	ns
t_{WI}	(1/2) T	MIN	ns
t_{HABE}	(1/2) T - 150	MAX	ns
t_{KKH} ($\overline{SCK}$ Output)	(1/2) (2T - 109)	MIN	ns
t_{KKL} ($\overline{SCK}$ Output)	(1/2) (2T - 109)	MIN	ns

Notes: ① N = Number of Wait States

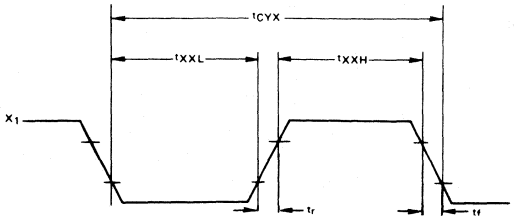
② T = $t_{CY\phi}$

③ Only above parameters are t_{CY_ϕ} dependent

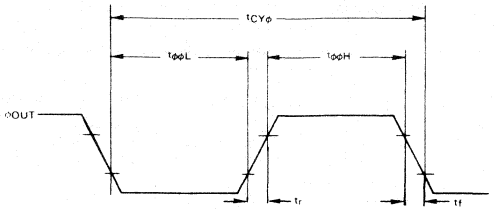
④ When a crystal frequency other than 4 MHz is used (t_{CY_ϕ} = 500 ns) the above equations can be used to calculate AC parameter values.

CLOCK TIMING

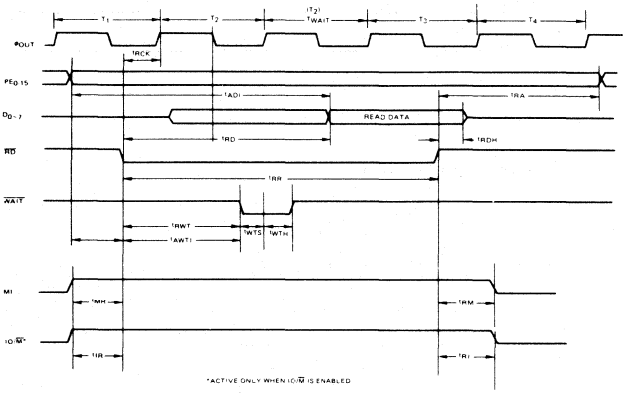
TIMING WAVEFORMS



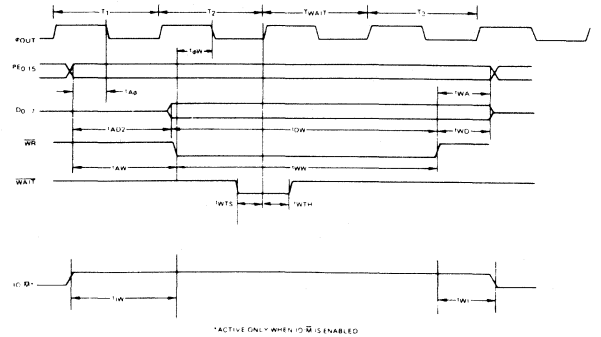
TIMING WAVEFORMS (CONT.)



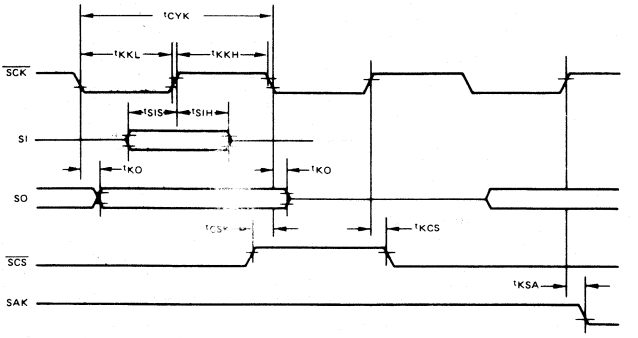
READ OPERATION



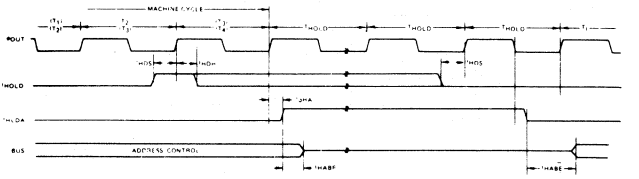
WRITE OPERATION



SERIAL I/O OPERATION



HOLD OPERATION



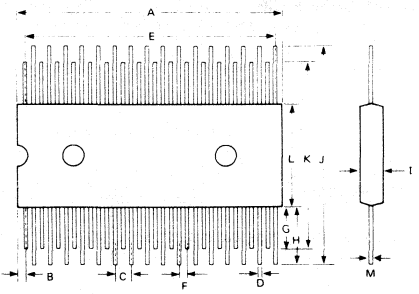
PACKAGE OUTLINES

Plastic Quil, μPD7801G/02G
Plastic Shrinkdip, μPD7801CW, μPD7802CW

64-PIN QUIL, STRAIGHT LEADS

PACKAGE OUTLINE

μPD7801G-xxx-37
μPD7802G-xxx-37

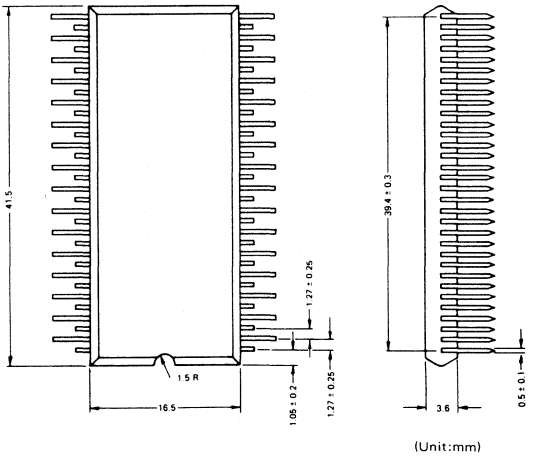


(Plastic)

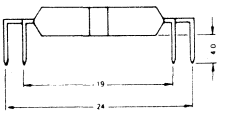
ITEM	MILLIMETERS	INCHES
A	41.8 MAX.	1.65
B	1.22	0.05
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	39.37	1.55
F	1.27	0.05
G	6.75	0.27
H	9.3	0.37
I	3.6	0.14
J	36.1	1.38
K	30.0	1.18
L	16.5	0.65
M	0.25 ± 0.05	0.01 ± 0.002

64-PIN QUIL, BENT LEADS

μPD7800G-36
μPD7801G-xxx-36
μPD7802G-xxx-36



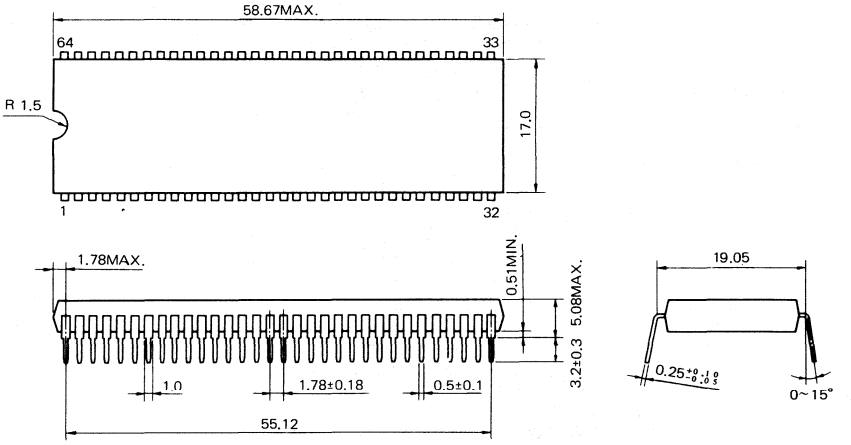
(Unit:mm)



PACKAGE OUTLINE

64-PIN SHRINK DIP

μPD7801CW-xxx
μPD7802CW-xxx



ELECTRICAL SPECIFICATIONS FOR EXTENDED TEMPERATURE RANGE OF -40 °C TO +85 °C μPD7800/μPD7801/μPD7802

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −40°C to +85°C
Storage Temperature . . . . . −65°C to +125°C
Voltage On Any Pin . . . . . −0.3V to +7.0V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −40 ~ +85°C, V_{CC} = +5.0V ± 10 %

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	0		0.7	V	
Input High Voltage	V_{IH1}	2.3		V_{CC}	V	Except $\overline{SCK}$, X1
	V_{IH2}	3.8		V_{CC}	V	$\overline{SCK}$, X1
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −100 μA
	V_{OH2}	2.0			V	I_{OH} = −500 μA
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_{IN} = 0V
High Level Input Leakage Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = 0.45V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Power Supply Current	I_{CC}		110	220	mA	

CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_I			10	pF	fc = 1 MHz All pins not under test at 0V
Output Capacitance	C_O			20	pF	
Input/Output Capacitance	C_{IO}			20	pF	

AC CHARACTERISTICS

CLOCK TIMING

T_a = −10 to +70°C, V_{CC} = +5.0V ± 10 %

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
X_{OUT} Cycle Time	t_{CYX}	666	2000	ns	t_{CYX}
X_{OUT} Low Level Width	t_{XXL}	256		ns	t_{XXL}
X_{OUT} High Level Width	t_{XXH}	256		ns	t_{XXH}

READ/WRITE OPERATION

AC CHARACTERISTICS (CONT.)

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
$\overline{RD}$ L.E. → X_{OUT} L.E.	t_{RX}	20		ns	
Address (PE_{0-15}) → Data Input	t_{AD1}		550 + 500 x N	ns	
$\overline{RD}$ T.E. → Address	t_{RA}	200(T3); 700(T4)		ns	
$\overline{RD}$ L.E. → Data Input	t_{RD}		350 + 500 x N	ns	
$\overline{RD}$ T.E. → Data Hold Time	t_{RDH}	0		ns	
$\overline{RD}$ Low Level Width	t_{RR}	850 + 500 x N		ns	
$\overline{RD}$ L.E. → $\overline{WAIT}$ L.E.	t_{RWT}		450	ns	
Address (PE_{0-15}) → WAIT L.E.	t_{AWT1}		650	ns	
$\overline{WAIT}$ Set Up Time (Referenced from X_{OUT} L.E.)	t_{WTS}	180		ns	
$\overline{WAIT}$ Hold Time (Referenced from X_{OUT} L.E.)	t_{WTH}	0		ns	
M1 → $\overline{RD}$ L.E.	t_{MR}	200		ns	t_{CYX} = 500 ns
$\overline{RD}$ T.E. → M1	t_{RM}	200		ns	
IO/$\overline{M}$ → $\overline{RD}$ L.E.	t_{IR}	200		ns	
$\overline{RD}$ T.E. → IO/$\overline{M}$	t_{RI}	200		ns	
X_{OUT} L.E. → WR L.E.	t_{XW}		270	ns	
Address (PE_{0-15}) → X_{OUT} T.E.	t_{AX}		300	ns	
Address (PE_{0-15}) → Data Output	t_{AD2}	450		ns	
Data Output → $\overline{WR}$ T.E.	t_{DW}	600 + 500 x N		ns	
$\overline{WR}$ T.E. → Data Stabilization Time	t_{WD}	150		ns	
Address (PE_{0-15}) → $\overline{WR}$ L.E.	t_{AW}	400		ns	
$\overline{WR}$ T.E. → Address Stabilization Time	t_{WA}	200		ns	
$\overline{WR}$ Low Level Width	t_{WW}	600 + 500 x N		ns	
IO/$\overline{M}$ → $\overline{WR}$ L.E.	t_{IW}	500		ns	
$\overline{WR}$ T.E. → IO/$\overline{M}$	t_{WI}	250		ns	

AC CHARACTERISTICS (CONT.)

SERIAL I/O OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
$\overline{SCK}$ Cycle Time	t_{CYK}	800		ns	$\overline{SCK}$ Input
		700	4000	ns	$\overline{SCK}$ Output
$\overline{SCK}$ Low Level Width	t_{KKL}	350		ns	$\overline{SCK}$ Input
		300		ns	$\overline{SCK}$ Output
$\overline{SCK}$ High Level Width	t_{KKH}	350		ns	$\overline{SCK}$ Input
		300		ns	$\overline{SCK}$ Output
SI Set-Up Time (referenced from $\overline{SCK}$ T.E.)	t_{SIS}	140		ns	
SI Hold Time (referenced from $\overline{SCK}$ T.E.)	t_{SIH}	260		ns	
$\overline{SCK}$ L.E. → SO Delay Time	t_{KO}		180	ns	
$\overline{SCS}$ High → $\overline{SCK}$ L.E.	t_{CSK}	100		ns	
$\overline{SCK}$ T.E. → $\overline{SCS}$ Low	t_{KCS}	100		ns	
$\overline{SCK}$ T.E. → SAK Low	t_{KSA}		260	ns	

PEN, PEX, PER OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
X_1 L.E. → $\overline{EXT}$	t_{XE}		250	ns	t_{CYX} = 500 ns
Address (AB_{0-15}) → STB L.E.	t_{AST}	200			
Data (DB_{0-7}) → STB L.E.	t_{DST}	200			
STB Hold Time	t_{STST}	300			
STB → Data	t_{STD}	400			

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from X_{OUT} L.E.)	t_{HDS_1}	100		ns	
	t_{HDS_2}	100		ns	
HOLD Hold Time (referenced from $\emptyset_{OUT}$ L.E.)	t_{HDH}	100		ns	
X_{OUT} L.E. → HLDA	t_{XHA}		100	ns	
HLDA High → Bus Floating (High Z State)	t_{HABF}	−150	150	ns	
HLDA Low → Bus Enable	t_{HABE}		350	ns	

Notes:

① AC Signal waveform (unless otherwise specified)

② Output Timing is measured with 1 TTL + 200 pF measuring points are V_{OH} = 2.0V
V_{OL} = 0.8V

③ L.E. = Leading Edge, T.E. = Trailing Edge

AC CHARACTERISTICS (CONT.)

t_{CYX} DEPENDENT AC PARAMETERS

PARAMETER	EQUATION	MIN/MAX	UNIT
t_{RX}	(1/25) T	MIN	ns
t_{AD_1}	(3/2 + N) T - 200	MAX	ns
t_{RA} (T_3)	(1/2) T - 50	MIN	ns
t_{RA} (T_4)	(3/2) T - 50	MIN	ns
t_{RD}	(1 + N) T - 150	MAX	ns
t_{RR}	(2 + N) T - 150	MIN	ns
t_{RWT}	(3/2) T - 300	MAX	ns
t_{AWT_1}	(2) T - 350	MAX	ns
t_{MR}	(1/2) T - 50	MIN	ns
t_{RM}	(1/2) T - 50	MIN	ns
t_{IR}	(1/2) T - 50	MIN	ns
t_{RI}	(1/2) T - 50	MIN	ns
t_{XW}	(27/50) T	MAX	ns
t_{AD_2}	T - 50	MIN	ns
t_{DW}	(3/2 + N) T - 150	MIN	ns
t_{WD}	(1/2) T - 100	MIN	ns
t_{AW}	T - 100	MIN	ns
t_{WA}	(1/2) T - 50	MIN	ns
t_{WW}	(3/2 + N) T - 150	MIN	ns
t_{IW}	T	MIN	ns
t_{WI}	(1/2) T	MIN	ns
t_{HABE}	(1/2) T - 150	MAX	ns
t_{AST}	(2/5) T	MIN	ns
t_{DST}	(2/5) T	MIN	ns
t_{STST}	(3/5) T	MIN	ns
t_{STD}	(4/5) T	MIN	ns

Notes: ① N = Number of Wait States

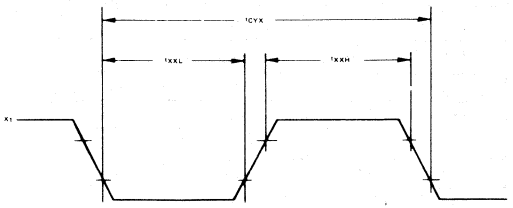
② T = t_{CYX}

③ Only above parameters are t_{CYX} dependent

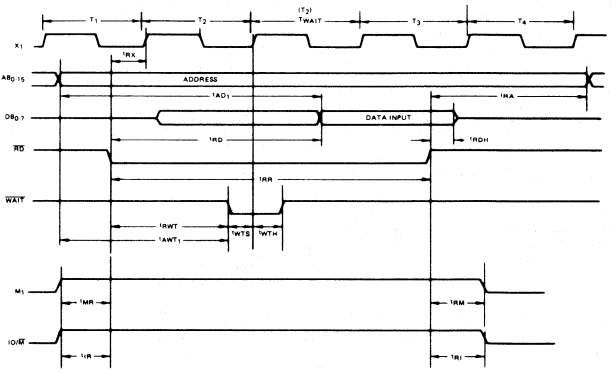
④ When a crystal frequency other than 4 MHz is used (t_{CYX} = 500 ns) the above equations can be used to calculate AC parameter values.

TIMING WAVEFORMS

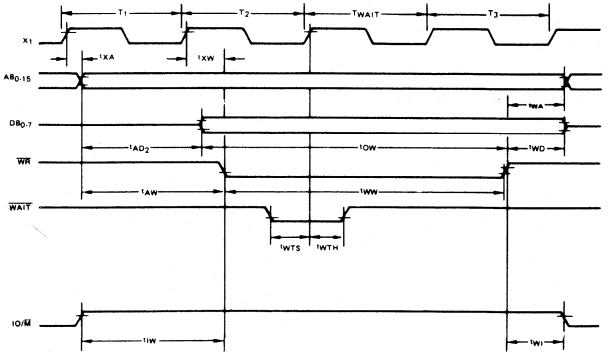
CLOCK TIMING



READ OPERATION



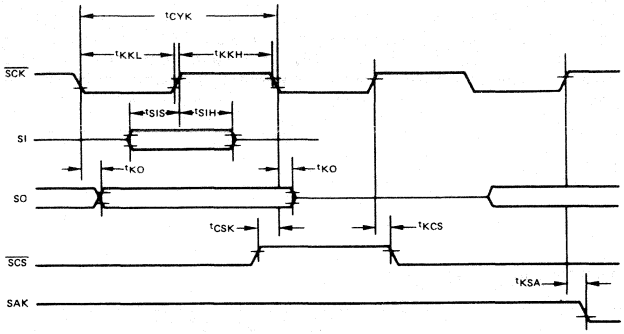
WRITE OPERATION



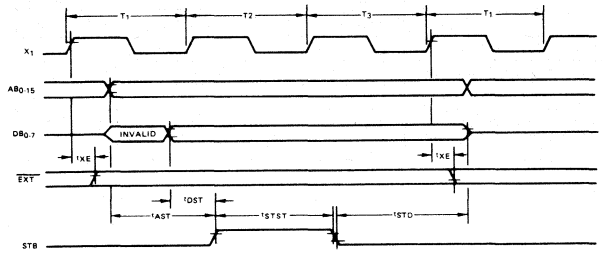
** $\overline{WAIT}$ should be supplied with VOH or VOL during t_{WTS} and t_{WTH}, otherwise malfunction may occur.

TIMING WAVEFORMS (CONT.)

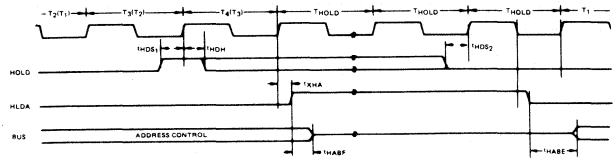
SERIAL I/O OPERATION



PEN, PEX, PER OPERATION



HOLD OPERATION



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −40°C to +85°C
Storage Temperature . . . . . −65°C to +125°C
Voltage On Any Pin . . . . . −0.3V to +7.0V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above thos indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

−10 to +70°C, V_{CC} = +5.0V ± 10 %

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	0		0.7	V	
Input High Voltage	V_{IH1}	2.3		V_{CC}	V	Except $\overline{SCK}$, X1
	V_{IH2}	3.8		V_{CC}	V	$\overline{SCK}$, X1
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −100 μA
	V_{OH2}	2.0			V	I_{OH} = −500 μA
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_{IN} = 0V
High Level Input Leakage Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = 0.45V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Power Supply Current	I_{CC}		110	220	mA	

CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_I			10	pF	fc = 1 MHz All pins not under test at 0V
Output Capacitance	C_O			20	pF	
Input/Output Capacitance	C_{IO}			20	pF	

CLOCK TIMING

AC CHARACTERISTICS

-10 to $+70°C$, $V_{CC} = +5.0V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
X1 Input Cycle Time	t_{CYX}	333	1000	ns	
X1 Input Low Level Width	t_{XXL}	159		ns	
X1 Input High Level Width	t_{XXH}	159		ns	
ϕ_{OUT} Cycle Time	$t_{CY\phi}$	666	2000	ns	
ϕ_{OUT} Low Level Width	$t_{\phi\phi L}$	256		ns	
ϕ_{OUT} High Level Width	$t_{\phi\phi H}$	256		ns	
ϕ_{OUT} Rise/Fall Time	t_{r}, t_{f}		40	ns	

READ/WRITE OPERATION

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
$\overline{RD}$ L.E. → ϕ_{OUT} L.E.	$t_{R\phi}$	100		ns	
Address ($PE_{0\text{-}15}$) → Data Input	t_{AD1}		550 + 500 x N	ns	
$\overline{RD}$ T.E. → Address	t_{RA}	200(T3); 700(T4)		ns	
$\overline{RD}$ L.E. → Data Input	t_{RD}		350 + 500 x N	ns	
$\overline{RD}$ T.E. → Data Hold Time	t_{RDH}	0		ns	
$\overline{RD}$ Low Level Width	t_{RR}	850 + 500 x N		ns	
$\overline{RD}$ L.E. → $\overline{WAIT}$ L.E.	t_{RWT}		450	ns	
Address ($PE_{0\text{-}15}$) → WAIT L.E.	t_{AWT1}		650	ns	
$\overline{WAIT}$ Set Up Time (Referenced from ϕ_{OUT} L.E.)	t_{WTS}	290		ns	
$\overline{WAIT}$ Hold Time (Referenced from ϕ_{OUT} L.E.)	t_{WTH}	0		ns	
M1 → $\overline{RD}$ L.E.	t_{MR}	200		ns	$t_{CY\phi}$ = 500 ns
$\overline{RD}$ T.E. → M1	t_{RM}	200		ns	
IO/$\overline{M}$ → $\overline{RD}$ L.E.	t_{IR}	200		ns	
$\overline{RD}$ T.E. → IO/$\overline{M}$	t_{RI}	200		ns	
ϕ_{OUT} L.E. → $\overline{WR}$ L.E.	$t_{\phi W}$	40	125	ns	
Address ($PE_{0\text{-}15}$) → ϕ_{OUT} T.E.	$t_{A\phi}$	100	300	ns	
Address ($PE_{0\text{-}15}$) → Data Output	t_{AD2}	450		ns	
Data Output → $\overline{WR}$ T.E.	t_{DW}	600 + 500 x N		ns	
$\overline{WR}$ T.E. → Data Stabilization Time	t_{WD}	150		ns	
Address ($PE_{0\text{-}15}$) → $\overline{WR}$ L.E.	t_{AW}	400		ns	
$\overline{WR}$ T.E. → Address Stabilization Time	t_{WA}	200		ns	
$\overline{WR}$ Low Level Width	t_{WW}	600 + 500 x N		ns	
IO/$\overline{M}$ → $\overline{WR}$ L.E.	t_{IW}	500		ns	
$\overline{WR}$ T.E. → IO/$\overline{M}$	t_{WI}	250		ns	

SERIAL I/O OPERATION

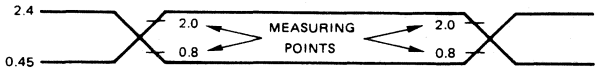
PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
$\overline{SCK}$ Cycle Time	t_{CYK}	800		ns	$\overline{SCK}$ Input
		700	4000	ns	$\overline{SCK}$ Output
$\overline{SCK}$ Low Level Width	t_{KKL}	350		ns	$\overline{SCK}$ Input
		300		ns	$\overline{SCK}$ Output
$\overline{SCK}$ High Level Width	t_{KKH}	350		ns	$\overline{SCK}$ Input
		300		ns	$\overline{SCK}$ Output
SI Set-Up Time (referenced from $\overline{SCK}$ T.E.)	t_{SIS}	140		ns	
SI Hold Time (referenced from $\overline{SCK}$ T.E.)	t_{SIH}	260		ns	
$\overline{SCK}$ L.E. → SO Delay Time	t_{KO}		180	ns	
$\overline{SCS}$ High → $\overline{SCK}$ L.E.	t_{CSK}	100		ns	
$\overline{SCK}$ T.E. → $\overline{SCS}$ Low	t_{KCS}	100		ns	
$\overline{SCK}$ T.E. → SAK Low	t_{KSA}		260	ns	

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from ϕ_{OUT} L.E.)	t_{HDS_1}	200		ns	$t_{CY\phi}$ = 500 ns
	t_{HDS_2}	200		ns	
HOLD Hold Time (referenced from ϕ_{OUT} L.E.)	t_{HDH}	0		ns	
ϕ_{OUT} L.E. → HLDA	t_{DHA}	110	100	ns	
HLDA High → Bus Floating (High Z State)	t_{HABF}	−150	150	ns	
HLDA Low → Bus Enable	t_{HABE}		350	ns	

Notes:

① AC Signal waveform (unless otherwise specified)



② Output Timing is measured with 1 TTL + 200 pF measuring points are V_{OH} = 2.0V
V_{OL} = 0.8V

③ L.E. = Leading Edge, T.E. = Trailing Edge

AC CHARACTERISTICS (CONT.)

$t_{CY\phi}$ DEPENDENT AC PARAMETERS

PARAMETER	EQUATION	MIN/MAX	UNIT
$t_{R\phi}$	(1/5) T	MIN	ns
t_{AD_1}	(3/2 + N) T - 200	MAX	ns
t_{RA} (T_3)	(1/2) T - 50	MIN	ns
t_{RA} (T_4)	(3/2) T - 50	MIN	ns
t_{RD}	(1 + N) T - 150	MAX	ns
t_{RR}	(2 + N) T - 150	MIN	ns
t_{RWT}	(3/2) T - 300	MAX	ns
t_{AWT_1}	(2) T - 350	MAX	ns
t_{MR}	(1/2) T - 50	MIN	ns
t_{RM}	(1/2) T - 50	MIN	ns
t_{IR}	(1/2) T - 50	MIN	ns
t_{RI}	(1/2) T - 50	MIN	ns
$t_{\phi W}$	(1/4) T	MAX	ns
$t_{A\phi}$	(1/5) T	MIN	ns
t_{AD_2}	T - 50	MIN	ns
t_{DW}	(3/2 + N) T - 150	MIN	ns
t_{WD}	(1/2) T - 100	MIN	ns
t_{AW}	T - 100	MIN	ns
t_{WA}	(1/2) T - 50	MIN	ns
t_{WW}	(3/2 + N) T - 150	MIN	ns
t_{IW}	T	MIN	ns
t_{WI}	(1/2) T	MIN	ns
t_{HABE}	(1/2) T - 150	MAX	ns

Notes: ① N = Number of Wait States

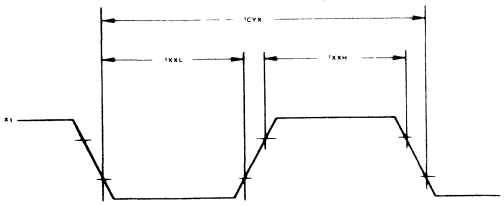
② $T = t_{CY\phi}$

③ Only above parameters are t_{CY_ϕ} dependent

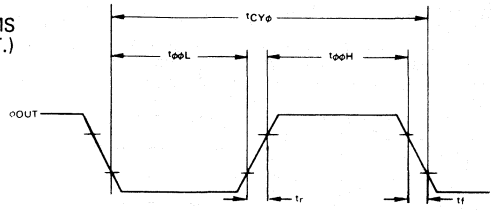
④ When a crystal frequency other than 4 MHz is used (t_{CY_ϕ} = 500 ns) the above equations can be used to calculate AC parameter values.

CLOCK TIMING

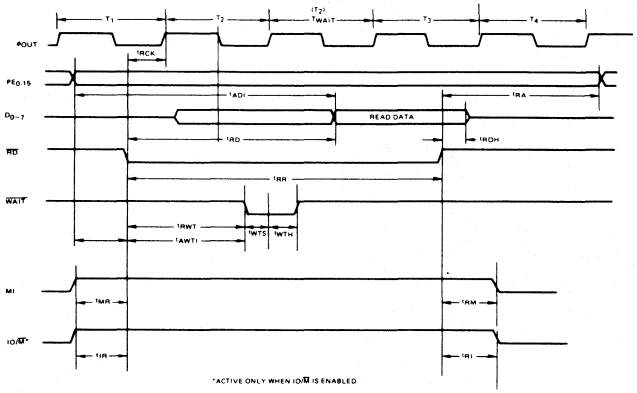
TIMING WAVEFORMS



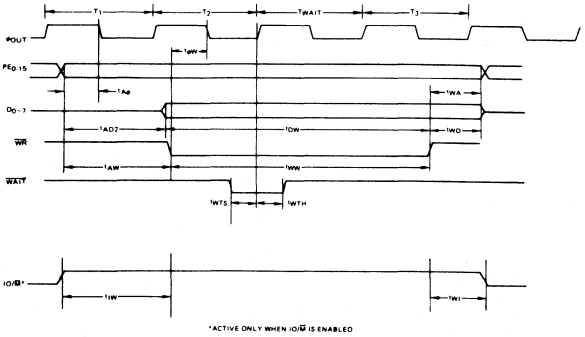
TIMING WAVEFORMS (CONT.)



READ OPERATION

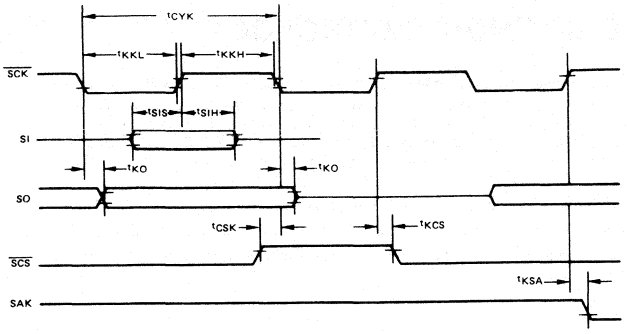


WRITE OPERATION

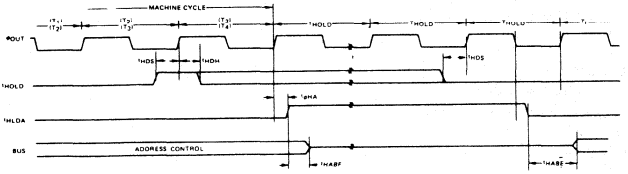


** $\overline{WAIT}$ should be supplied with VOH or VOL during t_{WTS} and t_{WTH}, otherfrise malfuncti
may occur.

SERIAL I/O OPERATION



HOLD OPERATION



HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER ROM-LESS DEVELOPMENT DEVICE IN CMOS TECHNOLOGY

DESCRIPTION

The μPD78C05A is a high-performance 8-bit microcomputer fabricated with CMOS technology. The μPD78C05A contains an 8-bit ALU, a 128 x 8 RAM, two 8-bit I/O ports, a 6-bit I/O port, an 8-bit timer/event counter with 4-bit prescaler, a serial I/O port, and three (two external and one internal) source vectored interrupt structure. It also contains a 16-bit Address bus and an 8-bit data bus for external memory (program memory, data memory, or memory mapped I/O) up to 64K bytes.

The μPD78C05A has stand-by capability (STOP/HALT) for its power-down.

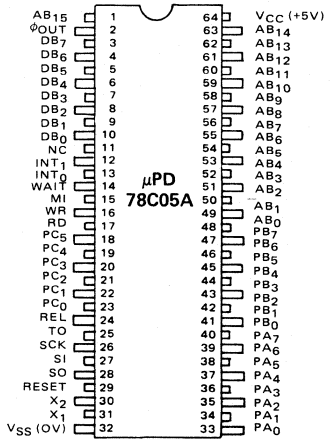
The μPD78C05A is applicable for hand-held computer, etc. requiring low power consumption.

The μPD78C05A is compatible with the μPD78C06A (μCOM-87LC-family) and used as evaluation chip for μCOM-87LC-series.

FEATURES

- Powerful 101 Instructions
- Instruction Cycle Time: 2,6 μs for 78C05A,
- Data Memory: 128W x 8
- Direct Addressing Capability up to 64kB External Memory
- Powerful Addressing Modes Capability
- Multi-level Stack
- Vectored Interrupts (External: 2, Internal: 1)
- On-chip 8-bit Timer with 4-bit Prescaler
- 46 I/O Ports
- Serial I/O Ports
- Stand-by Capability (STOP/HALT mode)
- Fully Bus Compatible with 8080A
- On-chip Clock Generator with 6 MHz crystal
- Single Supply, CMOS Technology
- Low Power Consumption
- 64 pin QUIL
- μPD78C06A Evaluation chip

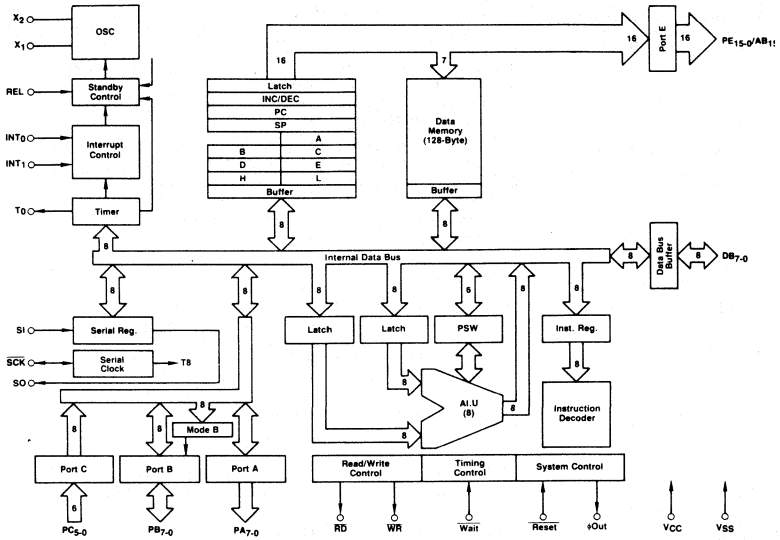
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	DESIGNATION	FUNCTION
1, 49-63	AB_0-AB_{15}	(Output), 16 bit address bus and output port.
2	ϕOUT	(Output) The clock of system clock frequency (1/4 of crystal frequency or X_1 external clock frequency) is placed out from this line. It is still placed out in HALT mode, but it is fixed to high in STOP mode.
3-10	DB_7-DB_0	(Tri-State Input/Output) This is an 8-bit bi-directional data bus. The data move between an external memory or I/O STOP, and accumulator is done through this data bus. During an input, HALT, and RESET, the output of the data bus goes a high impedance state. Input/Output level are TTL compatible.
12	INT_0	(Input) It is a level-sensitive interrupt input line which is high level active.
13	INT_1	(Input) It is a rising-edge sensitive interrupt line, and it becomes valid when INT_1 input goes low to high. Subsequently, if users want to perform another interrupt on this line after an interrupt on this line is accepted, they must take it into consideration that INT_1 input should be maintained at low state a little while, and then it should go high. Unless, it does not enable another interrupt.
14	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state T_W and remains in that state as long as $\overline{WAIT}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-23	PC_0-PC_5	(Input) This is a 6-bit input port with pull-up resistors. Input data to this port can be test by test instruction, and also moved to least significant 6-bit of accumulator. Input level is CMOS compatible. This port is fit for key-input port.
24	REL	(Input) This is an input to release the STOP mode of stand-by function. STOP mode is released by raising the REL input high, then clock generator which has been stopped will restart. During REL input is high, the bit 3 of Stand-by Control Register (SC3) is set to one, and it is reset to zero after REL signal returns low. Pull-down resistor is built in.
25	TO	(Output) The square wave is output from this line. Its cycle time is half of a count time of the internal timer. It goes on low level after reset.
26	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of SCK.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of SCK, MSB to LSB.
29	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD78C05A
30	X_2	(Output) Oscillator output.
31	X_1	(Input) Clock Input
33-40	PA_0-PA_7	(Output) 8-bit output port with latch capability.
41-48	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

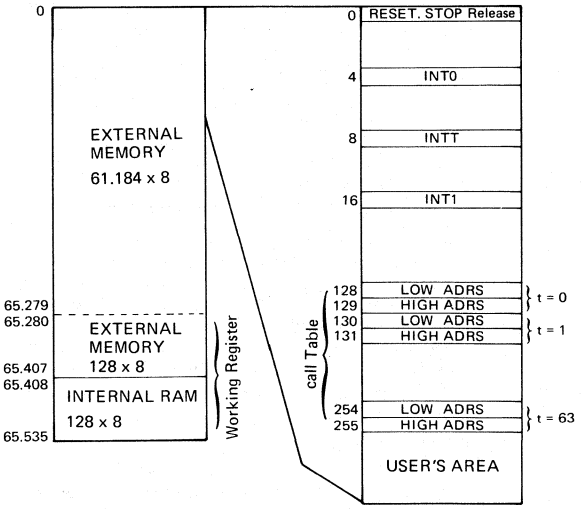
BLOCK DIAGRAM



Memory Map

The μPD78C05A can directly address the memory up to 64k bytes. Except on-chip RAM (65.408-65.535) any memory location can be used as either of RAM or ROM, freely. The memory map of the μPD78C05A is shown on the next page. In the specific memory area, the Reset/Stop mode Restart Address, Interrupt Start Address, Call Table etc. are involved. External memory (ROM), and/or working registers, freely.

FUNCTIONAL DESCRIPTION



HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH 4K ROM IN CMOS TECHNOLOGY

DESCRIPTION

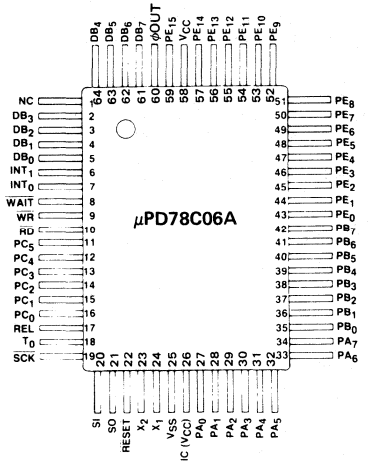
The NEC μPD78C06A is a general purpose single-chip microcomputer. The μPD78C06A is fabricated with CMOS technology.

This contains the functional blocks of program memory, data memory, ALU, I/O ports, on-chip timer, serial I/O and internal clock generator. It can extend external memory capacity (ROM, RAM) up to 60k bytes.

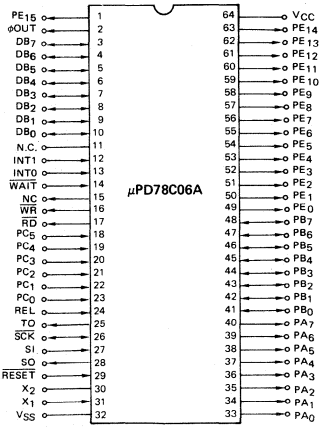
FEATURES

- Single-chip Microcomputer (μCOM-87LC)
- Powerful 101 Instructions
- Instruction Cycle Time: 4 μs (on-chip ROM); 2,6 μs (external memory & on-chip RAM) } for 78C06A
- Program Memory (ROM): 4096W x 8
- Data Memory (RAM): 128W x 8
- Direct Addressing Capability up to 60kB External Memory
- Powerful Addressing Modes Capability
- Multi-level Stack
- Vectored Interrupts (External: 2, Internal: 1)
- On-chip 8-bit Timer with 4-bit Prescaler
- 46 I/O Ports
- Serial I/O Ports
- Stand-by Capability (STOP/HALT mode)
- Fully Bus Compatible with 8080A
- On-chip Clock Generator
- Single Supply, CMOS Technology
- Low Power Consumption
- 64 pin Plastic Flat Package
- 64 pin Quil

PIN CONFIGURATION



(Top View)

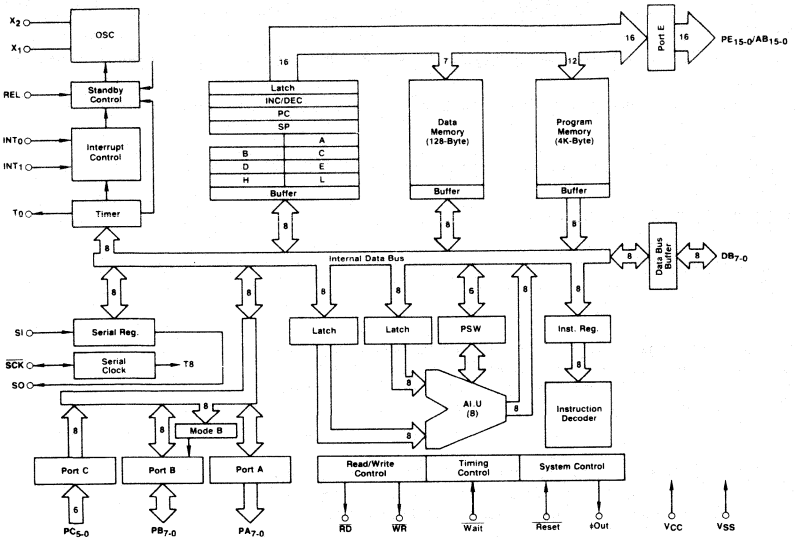


NC: Non-connection

PIN DESCRIPTION

PIN NO.	DESIGNATION	FUNCTION
2-5 61-64	DB_0-DB_7	(Input/Output) This is an 8-bit bi-directional data bus. The data move between an external memory or I/O, and accumulator is done through this data bus. During an input, HALT, STOP mode, and RESET, the output of the data bus goes a high impedance state. Input/Output level are TTL compatible.
6	INT_1	(Input) It is a rising-edge sensitive interrupt line, and it becomes valid when INT_1 input goes low to high. Subsequently, if users want to perform another interrupt on this line after an interrupt on this line is accepted, they must take it into consideration that INT_1 input should be maintained at low state a little while, and then it should go high. Unless, it does not enable another interrupt.
7	INT_0	(Input) It is a level-sensitive interrupt input line which is high level active.
8	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state T_W and remains in that state as long as $\overline{WAIT}$ is active.
9	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
10	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
11-16	PC_0-PC_5	(Input) This is a 6-bit input port with pull-up resistors. Input data to this port can be test by test instruction, and also moved to least significant 6-bit of accumulator and higher 2-bit of accumulator is lodaded with "0". Input level is CMOS compatible. This port is fit for key-input port.
17	REL	(Input) This is an input to release the STOP mode of stand-by function. STOP mode is released by raising the REL input high, then clock generator which has been stopped will restart. During REL input is high, the bit 3 of Stand-by Control Register (SC3) is set to one, and it is reset to zero after REL signal returns low. Pull-down resistor is built in.
18	TO	(Output) The square wave is output from this line. Its cycle time is half of a count time of the internal timer. It goes on low level after reset.
19	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
20	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of SCK.
22	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of SCK, MSB to LSB.
22	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD78C06A.
23	X_2	(Output) Oscillator output.
24	X_1	(Input) Clock Input
27-34	PA_0-PA_7	(Output) 8-bit output port with latch capability.
35-42	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.
43-57,59	PE_0-PE_{15}	(Output) 16-bit address bus and output port.
64	ϕOUT	(Output) The Clock of system clock frequency (1/8 of crystal frequency or X_1 external clock frequency) is placed out from this line. It is still placed out in HALT mode, but it is fixed to high in STOP mode.

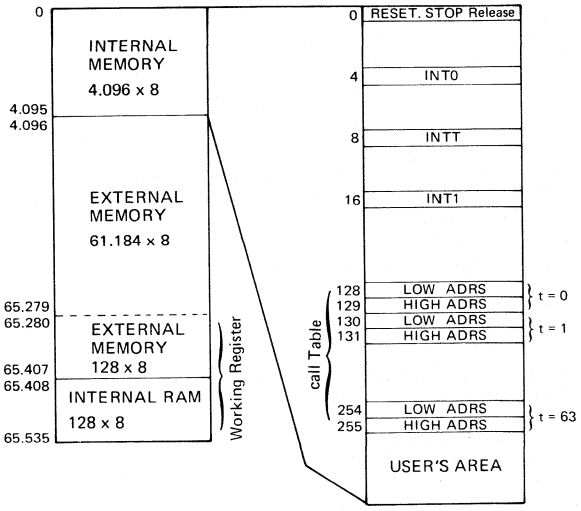
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Memory Map

The μPD78C06A can directly address the memory up to 64k bytes. Except on-chip ROM (0-4095) and RAM (65.408-65.535), and memory location can be used as either of RAM or ROM, freely. In the internal ROM area, the Reset/Stop mode Restart Address, Interrupt Start Address, Call Table etc. are involved. External memory and on-chip RAM area can be used as data memory (RAM), program memory (ROM), and/or working registers, freely.



FUNCTIONAL DESCRIPTION

I/O PORTS

PORT	FUNCTIONS
Port A	8-bit output port with latch
Port B	8-bit programmable Input/Output port w/latch
Port C	6-bit input port with pull up resistors
Port E	16-bit Address bus/Output Port

Port A

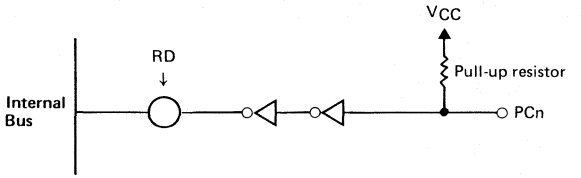
Port A is an 8-bit latched output port. Data can be readily transferred between the accumulator and the output latch buffers. The contents of the output latches can be modified using Arithmetic and Logic instructions. Data remains latched at Port A unless acted on by another Port A instruction or a RESET is issued.

Port B

Port B is an 8-bit I/O port. Data is latched at Port B in both the Input or Output modes. Each bit of Port B can be independently set to either Input or Output mode. The Mode B register programs the individual lines of Port B to be either an Input (Mode $B_n = 1$) or an Output (Mode $B_n = 0$).

Port C

This is a 6-bit input port with pull-up resistors. Input data to this port can be test by instruction, and also moved to least significant 6-bit of accumulator and higher 2-bit of accumulator is loaded with "0". Input level is CMOS compatible. This port is fit for key-input port.



Port E (μPD78C06A)

Port E is a 16-bit address bus/output port. There are two ways to use these lines:

a) 16-Bit Address Bus – the PER instruction sets this mode for use with external I/O or memory expansion (up to 60K bytes, externally).

b) 16-Bit Output Port – the PEX instruction sets Port E to a 16-bit output port. The contents of B and C registers appear on PE_{8-15} and PE_{0-7}, respectively.

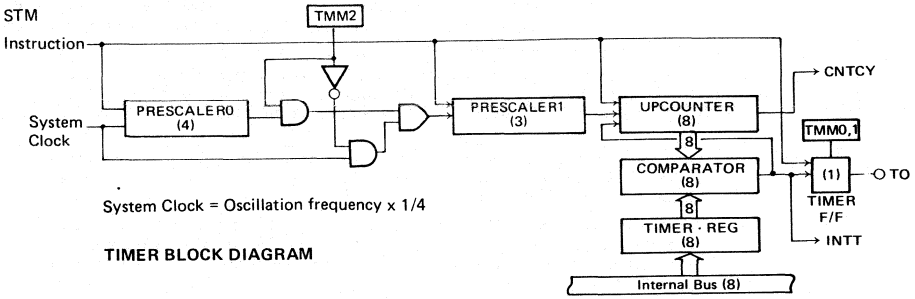
Address bus AB_{15}–AB_0 (μPD78C05A)

These lines are the 16 bit-to-bit address bus to the main memory. The μPD78C05A, having no internal ROM, must address the area from 0 to 4096 as external ROM.

The μPD78C05A AB lines are unlike the μPD78C06A PE lines; they have no internal latches. When the Port E output instruction PEX is executed in a μPD78C05A, the register pair BC is output to the AB lines for only one clock cycle during the third machine cycle. This is provided to allow external hardware to emulate the Port E operation of the μPD78C06A.

FUNCTIONAL DESCRIPTION (CONT.)

TIMER OPERATION



System Clock = Oscillation frequency x 1/4

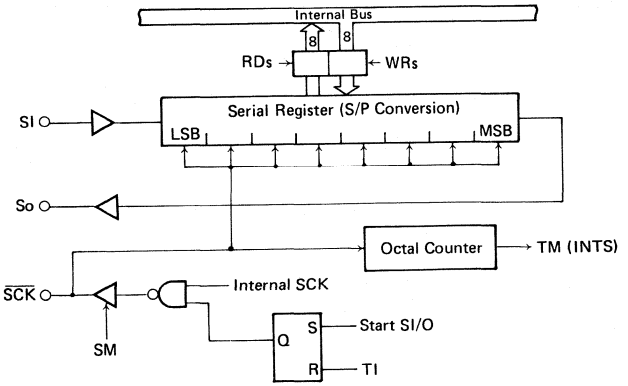
TIMER BLOCK DIAGRAM

This is a programmable 8-bit interval timer with prescaler. It consists of TIMER·REG (8-bit), PRESCALER0 (4-bit), PRESCALER1 (3-bit), UPCOUNTER (8-bit), COMPARATOR (8-bit), and TIMER F/F.

Count time and TO output are controlled by Timer Mode Register (TMM). It can count 5,3 μsec to 1,3 msec with resolution of 5,3 μsec (TMM2 = 0), or 85,3 μsec to 21,3 msec with resolution of 85,3 μsec (TMM2 = 1).

At first set the count value to the TIMER REG by MOV TM, A instruction, then initialize the PRESCALER0, 1, TIMER F/F, UPCOUNTER and start timer by STM instruction. UPCOUNTER is incremented at every 5,3 μs (TMM2 = 0) or 85,3 μs (TMM2 = 1(. COMPARATOR always compares the contents of UPCOUNTER with TIMER·REG, and it generates match signal (internal interrupt; INTT) when they are matched. The match signal clears the content of UPCOUNTER, and restarts the countup. Accordingly, this timer operates as the interval timer which generates repetitive interrupts with the interval of count time specified by count value of TIMER·REG. When a timer interrupt is generated in HALT mode, the HALT mode is released.

SERIAL PORT OPERATION



The Block Diagram of Serial Ports

FUNCTIONAL DESCRIPTION (CONT.)

Serial interface section consists of Serial Input (SI) line, Serial Output (SO) Line, Serial Clock ($\overline{SCK}$) input/output line, an 8-bit Serial Register (S/P), an octal counter, a R-S flip-flop used for transfer control, and some gates. When the bit 6 of Serial Mode Register (SM6) is 0, $\overline{SCK}$ becomes internal clock mode fixed to 1/8 of oscillator frequency (if fosc = 6MHz, then $\overline{SCK}$ is fixed to 780KHz), however, when the SM6 is 1, it becomes external clock mode, and operates with DC to 780KHz external clock. Accordingly, the transfer operation in internal clock mode is performed synchronously with constant frequency, and in external clock mode it performed synchronously with variable frequency.

A transmitting data is set to serial register by MOV S, A instruction, then the octal counter is reset and serial transfer is triggered by SIO instruction. At every falling edge of $\overline{SCK}$, the contents of serial register are shift, and shift-out data are placed to SO line with MSB as starting bit.

While the $\overline{SCK}$ is low the data on SI line is loaded in continuously, and then latched to serial register at the rising edge of the $\overline{SCK}$. Like this both the input and output of serial data are performed by same $\overline{SCK}$.

After occuring eight $\overline{SCK}$ pulses and completing 8-bit serial data transfer, the carry T8 is generated from the octal counter and it sets the interrupt request flag (INTFS). But μPD78C05A/06A has no serial interrupt, then INTFS is checked by only test instruction (SKNIT FS).

In internal $\overline{SCK}$ mode, as T8 signal resets the control flip-flop, the following transfer after completing 8-bit transfer are disabled until next SIO instruction will be given.

Accordingly, the data transfer should be restarted by SIO instruction with the next conditions. In case of data reception, after receiving the data from serial register by MOV A,S instruction, and in case of data transmission, after setting the data to serial register by MOV S,A instruction, data transmittion must be done by SIO instructions.

INTERRUPT STRUCTURE

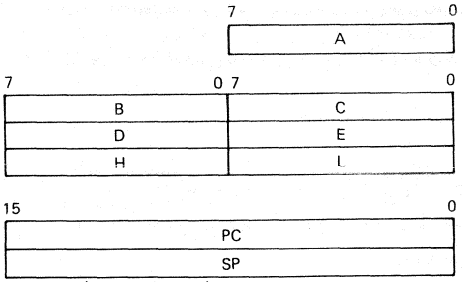
The μPD78C05A/06A provides a maskable interrupt structure capable of handling vectored prioritized interrupts. Interrupts can be generated from 3 different sources; two external interrupts and one internal interrupt. Each interrupt when activated branches to a designated memory vector location.

INT	VECTORED MEMORY LOCATION	PRIORITY	TYPE
INT_0	4	1	External, level sensitive
INT_1	16	3	External, rising edge sensitive
INTT	8	2	Internal, match on timer comparator

FUNCTIONAL DESCRIPTION (CONT.)

REGISTERS

This mainly consists of the seven 8-bit registers and two 16-bit registers as below.



General Purpose Registers (B, C, D, E, H, L)

They can function as auxilliary registers to the accumulator (A) or in pairs as data pointers (BC, DE, HL). Auto increment and decrement addressing mode capabilities extend the uses for the DE and HL register pairs.

Accumulator (A)

All data transfers between the μPD78C05A/06A and external memory or I/O are done through the accumulator. The contents of the Accumulator and Vector Registers can be exchanged with their Alternate Registers using the EX instruction.

Program Counter (PC)

The PC is a 16-bit register containing the address of the next instruction to be fetched. Under normal program flow, the PC is automatically incremented. However, in the case of a branch instruction, the PC contents are from another register or an instruction's immediate data. A Reset sets the PC to 0000_H.

Stack Pointer (SP)

The stack pointer is a 16-bit register used to maintain the top of the stack area (last-in-first-out). The contents of the SP are decremented during a CALL or PUSH instruction or if an interrupt occurs. The SP is incremented during a RETURN or POP instruction.

STAND-BY OPERATION

Stand-by function is used to lower the power consumption in stand-by condition, and there are two types of it: HALT mode and STOP mode.

In HALT mode the masking functions are active, so that programmer can chose an interrupt source, $\overline{\text{RESET}}$ or T8-signal for release use.

HALT AND STOP MODE

STOP mode can be released by REL or RESET signal. In both cases, program will start at location 0 again.

FUNCTION	HALT MODE	STOP MODE
Oscillator	Run	Stop
Internal System Clock	Stop	
Timer	Run	
Timer Register	Hold	Set
Upcounter, Prescaler 0, 1	Run	Cleared
Serial Interface		Run ①
Serial Clock	Hold	Hold
Interrupt Control Circuit	Run	Stop
Interrupt Enable Flag	Hold	Reset
INT_0, INT_1 Input	Active	Inactive
INT_T		–
T_8 (INTFS)		–
Mask Register	Hold	Set
Pending Interrupts (INTFX)		Reset
REL Input	Inactive	Active
$\overline{\text{RESET}}$ Input	Active	

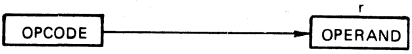
FUNCTION	HALT MODE	STOP MODE
On-chip RAM	Hold	Hold
Output Latch in Ports A, B, E		
Address Bus AB0 . . . 15		Low
Program Counter (PC)		Cleared
Stack Pointer (SP)		Unknown
General Registers (A, B, C, D, E, F, L)		
Program Status Word (PSW)		Reset
Mode B Register		Hold
Standby Control Register (SC_0–SC_3)		
Standby Control Register (SC_4)		Set
Timer Mode Register (TMM_0–TMM_1)		Hold
Timer Mode Register (TMM_1)		Set
Serial Mode Register (SM)		Hold
Data Bus (DB_0–DB_7)	High-Z	High-Z
$\overline{\text{RD}}$, $\overline{\text{WR}}$ Output	High	High

Note: ① Serial clock counter is running and T_8 is generated; however, there are no effects from it.

ADDRESS MODES

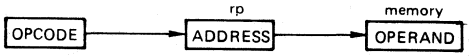
Register Addressing
Register Indirect Addressing
Auto-Increment Addressing
Auto-Decrement Addressing
Working Register Addressing
Direct Addressing
Immediate Addressing
Immediate Extended Addressing

Register Addressing



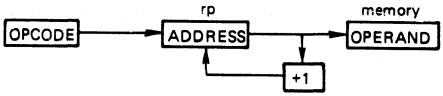
The instruction opcode specifies a register r which contains the operand.

Register Indirect Addressing



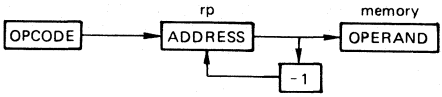
The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are ending this address mode.

Auto-Increment Addressing

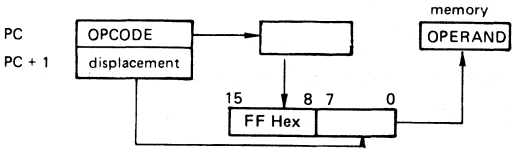


The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair is automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

Auto Decrement Addressing



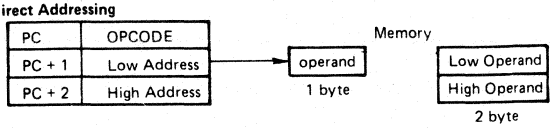
Working Register Addressing



The contents of the register is linked with the byte following the opcode to form a memory address whose contents is the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only 1 additional byte is required for the address. Mnemonics with a W suffix ending this address mode.

ADDRESS MODES (CONT.)

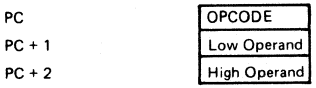
Direct Addressing



The two bytes following the opcode specify an address of a location containing the operand.

Immediate Addressing

Immediate Extended Addressing



PROGRAM STATUS WORD (PSW) OPERATION

OPERATION					D6	D5	D4	D3	D2	D0
REG. MEMORY		IMMEDIATE		SKIP	Z	SK	HC	L1	I0	CY
ADD ADC SUB SBB	ADDX ADCX SUBX SBBX	ADI ACI SUI SBI			‡	0	‡	0	0	‡
ANA ORA XRA	ANAX ORAX XRAX	ANI ORI XRI	ANIW ORIW		‡	0	•	0	0	•
ADDNC SUBNB GTA LTA	ADDNCX SUBNBX GTAX LTAX	ADINC SUINB GTI LTI	 LTIW		‡	‡	‡	0	0	‡
	ONAX OFFAX	ONI OFFI	ONIW OFFIW		‡	‡	•	0	0	•
NEA EQA	NEAX EQAX	NEI EQI	NEIW EQIW		‡	‡	‡	0	0	‡
INR DCR	INRW DCRW				‡	‡	‡	0	0	•
DAA					‡	0	‡	0	0	‡
RLL, RLR					•	0	•	0	0	‡
RLD – RRD					•	0	•	0	0	•
STC					•	0	•	0	0	1
CLC					•	0	•	0	0	0
		MVI A, byte			•	0	•	1	0	•
		MVI L, byte LXI H, word			•	0	•	0	1	•
				SKNC SKNZ SKNIT	•	‡	•	0	0	•
				RETS	•	1	•	0	0	•
All other instructions					•	0	•	0	0	•

Notes: ‡ Flag affected according to result op operation.
1 Flag set.
0 Flag reset.
• Flag not affected.

Symbols/Description on Operand

SYMBOLS	DESCRIPTIONS
r r1 r2	A, B, C, D, E, H, L B, C, D, E, H, L A, B, C
sr sr1 sr2	PA PB MK MB TM S TMM SM SC PA PB PC MK S TMM SC PA PB PC MK
rp rp1	SP, B, D, H V, B, D, H
rpa wa	B, D, H, D+, H+, D−, H− 8-bit immediate data
word byte bit	16-bit immediate data 8-bit immediate data 3-bit immediata data
if	F0, F1, FT, FS
f	CY, Z

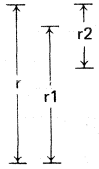
Notes:

1. At sr ~ sr2, the symbols of 'PA', 'PB', etc. stand for the following, respectively:
   PA = PORTA, PB = PORTB, PC = PORTC, MK = MASK·reg, MB = MODE·B, TM = TIMER·REG, S = SERIAL I/O, TMM = TIMER MODE REG, SM = SERIAL MODE REG, SC = STANDBY CONTROL REG
2. At rp ~ rp1, the 'SP', 'B', etc stand for the following, respectively;
   SP = STACK POINTER, B = BC, D = DE, H = HL, V = FFH·A
3. At rpa, the 'B', 'D', etc. stand for the following respectively:
   B = (BC), D = (DE), H = (HL), D+ = $(DE)^{+}$, H+ = $(HL)^{+}$, D− = $(DE)^{-}$, H− = $(HL)^{-}$
4. At if, the 'F0', 'F1', etc. stand for the following, respectively:
   F0 = INTF0, F1 = INTF1, FT = INTFT, FS = INTFS
5. At f, the 'CY', 'Z', stand for the following, respectively:
   CY = CARRY, Z = ZERO

The description of the symbols on Operation Codes is as follows:

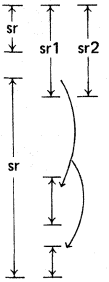
r

R_2	R_1	R_0	reg
0	0	0	
0	0	1	A
0	1	0	B
0	1	1	C
1	0	0	D
1	0	1	E
1	1	0	H
1	1	1	L



sr

S_3	S_2	S_1	S_0	special reg
0	0	0	0	PORT A
0	0	0	1	PORT B
0	0	1	0	PORT C
0	0	1	1	MASK
0	1	0	0	MODE-B
0	1	0	1	–
0	1	1	0	TIMER-REG
0	1	1	1	–
1	0	0	0	SERIAL-I/O
1	0	0	1	TIMER MODE REG
1	0	1	0	SERIAL MODE REG
1	0	1	1	STANDBY CONTROL REG

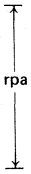


rp

P_1	P_0	reg-pair
0	0	SP
0	1	BC
1	0	DE
1	1	HL

rpa

A_2	A_1	A_0	addressing
0	0	0	–
0	0	1	(BC)
0	1	0	(DE)
0	1	1	(HL)
1	0	0	$(DE)^+$
1	0	1	$(HL)^+$
1	1	0	$(DE)^-$
1	1	1	$(HL)^-$



rp1

Q_1	Q_0	reg-pair
0	0	FFH.A
0	1	BC
1	0	DE
1	1	HL

if

I_2	I_1	I_0	INTF
0	0	0	INTF0
0	0	1	INTFT
0	1	0	INTF1
0	1	1	–
1	0	0	INTFS

f

F_2	F_1	F_0	flag
0	1	0	CY
1	0	0	Z

INSTRUCTION GROUPS

8-BIT DATA TRANSFER

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
MOV	r1, A	6	r1 ← A	
MOV	A, r1	6	A ← r1	
MOV	sr, A	14	sr ← A	
MOV	A, sr1	14	A ← sr1	
MOV	r, word	25	r ← (word)	
MOV	word, r	25	(word) ← r	
MVI	r, byte	11	r ← byte	
STAW	wa	14	(FFH, wa) ← A	
LDAW	wa	14	A ← (FFH, wa)	
STAX	rpa	9	(rpa) ← A	
LDAX	rpa	9	A ← (rpa)	
SBCD	word	28	(word) ← C, (word+1) ← B	
SDED	word	28	(word) ← E, (word+1) ← D	
SHLD	word	28	(word) ← L, (word+1) ← H	
SSPD	word	28	(word) ← SP_L, (word+1) ← SP_H	

16-BIT DATA TRANSFER

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
LBCD	word	28	C ← (word), B ← (word+1)	
LDED	word	28	E ← (word), D ← (word+1)	
LHLD	word	28	L ← (word), H ← (word+1)	
LSPD	word	28	SP_L ← (word), SP_H ← (word+1)	
PUSH	rp1	21	(SP−1) ← $rp1_H$, (SP−2) ← $rp1_L$	
POP	rp1	18	$rp1_L$ ← (SP), $rp1_H$ ← (SP+1) SP ← SP+2	
LXI	rp, word	16	rp ← word	

ARITHMETIC INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
ADD	A, r	12	A ← A+r	
ADDX	rpa	15	A ← A+(rpa)	
ADC	A, r	12	A ← A+r+CY	
ADCX	rpa	15	A ← A+(rpa)+CY	
SUB	A, r	12	A ← A−r	
SUBX	rpa	15	A ← A−(rpa)	
SBB	A, r	12	A ← A−r− CY	
SBBX	rpa	15	A ← A−(rpa)−CY	
ADDNC	A, r	12	A ← A+r	No Carry
ADDNCX	rpa	15	A ← A+(rpa)	No Carry
SUBNB	A, r	12	A ← A−r	No Borrow
SUBNBX	rpa	15	A ← A−(rpa)	No Borrow

LOGIC INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
ANA	A, r	12	A ← A∧r	
ANAX	rpa	15	A ← A∧(rpa)	
ORA	A, r	12	A ← A∨r	
ORAX	rpa	15	A ← A∨(rpa)	
XRA	A, r	12	A ← A∨r	
XRAX	rpa	15	A ← A∨(rpa)	
GTA	A, r	12	A−r−1	No Borrow
GTAX	rpa	15	A−(rpa)−1	No Borrow
LTA	A, r	12	A−r	Borrow
LTAX	rpa	15	A−(rpa)	Borrow
ONAX	rpa	15	A∧(rpa)	No Zero
OFFAX	rpa	15	A∧(rpa)	Zero
NEA	A, r	12	A−r	No Zero
NEAX	rpa	15	A−(rpa)	No Zero
EQA	A, r	12	A−r	Zero
EQAX	rpa	15	A−(rpa)	Zero

IMMEDIATE OPERATION INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
XRI	A, byte	11	A ← AVbyte	
DINC	A, byte	11	A ← A + byte	No Carry
SUINB	A, byte	11	A ← A−byte	No Borrow
ADI	A, byte	11	A ← A+byte	
ACI	A, byte	11	A ← A+byte+CY	
SUI	A, byte	11	A ← A−byte	
SBI	A, byte	11	A ← A−byte −CY	
ANI	A, byte	11	A ← A∧byte	
ORI	A, byte	11	A ← AVbyte	
GTI	A, byte	11	A−byte−1	No Borrow
LTI	A, byte	11	A−byte	Borrow
ONI	A, byte	11	A∧byte	No Zero
OFFI	A, byte	11	A∧byte	Zero
NEI	A, byte	11	A−byte	No Zero
EQI	A, byte	11	A−byte	Zero

SPECIAL REGISTER

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
ANI	sr2, byte	23	sr2 ← sr2∧byte	
ORI	sr2, byte	23	sr2 ← sr2Vbyte	
ONI	sr2, byte	20	sr2∧byte	No Zero
OFFI	sr2, byte	20	sr2∧byte	Zero

WORKING REGISTER OPERATIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
ANIW	wa, byte	22	(FFH.wa) ← (FFH.wa)∧byte	
ORIW	wa, byte	22	(FFH.wa) ← (FFH.wa)Vbyte	
GTIW	wa, byte	19	(FFH.wa)−byte−1 No Borrow	No Borrow
LTIW	wa, byte	19	(FFH.wa)−byte	Borrow
ONIW	wa, byte	19	(FFH.wa)∧byte	No Zero
OFFIW	wa, byte	19	(FFH.wa)∧byte	Zero
NEIW	wa, byte	19	(FFH.wa)−byte	No Zero
EQIW	wa, byte	19	(FFH.wa)−byte	Zero

INCREMENT/DECREMENT INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
INR	r2	6	r2 ← r2+1	Carry
INRW	wa	17	(FFH.wa) ← (FFH.wa)+1	Carry
DCR	r2	6	r2 ← r2–1	Borrow
DCRW	wa	17	(FFH.wa) ← (FFH.wa)–1	Borrow
INX	rp	9	rp ← rp+1	
DCX	rp	9	rp ← rp–1	

OTHER OPERATIONAL INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
DAA		6	Decimal Adjust Accumulator	
STC		12	CY ← 1	
CLC		12	CY ← 0	

ROTATION INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
RLD		21	Rotate Left Digit	
RRD		21	Rotate Right Digit	
RLL	A	12	Am+1 ← Am, A_0 ← CY, CY ← A_7	
RLR	A	12	Am–1 ← Am, A_7 ← CY, CY ← A_0	

JUMP INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
JMP	word	16	PC ← word	
JB		6	PC_H ← B PC_L ← C	
JR	word	12	PC ← PC+1+jdisp1	
JRE	word	17	PC ← PC+2+jdisp	

CALL INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
CALL	word	22	(SP–1) ← $(PC+3)_H$, (SP–2) ← $(PC+3)_L$, PC ← word	
CALF	word	17	(SP–1) ← $(PS+2)_H$, (SP–2) ← $(PC+2)_L$ PC15~11 ← 00001, PC10~0 ← 1a	
CALT	word	21	(SP–1) ← $(PC+1)_H$, (SP–2) → $PC+1)_L$ PC_L ← (128+21a), PC_H ← (129+21a)	

RETURN INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
RET		12	$PC_L \leftarrow (SP), PC_H \leftarrow (SP+1)$ $SP \leftarrow SP+2$	
RETS		12+n	$PC_L \leftarrow (SP), PC_H \leftarrow (SP+1), SP \leftarrow SP+2$ $PC \leftarrow PC+n$	Uncon-ditional Skip
RETI		15	$PC_L \leftarrow (SP), PC_H \leftarrow (SP+1)$ $PSW \leftarrow (SP+2), SI' \leftarrow SP+3$	

SKIP INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
SKN	CY	12	Skip if No Carry	CY = 0
SKN	Z	12	Skip if No Zero	Z = 0
SKNIT	if	12	Skip if No INTX Reset INTX if INTX = 1	f = 0

CPU CONTROL INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
NOP		6	No Operation	
EI		12	Enable Interrupt	
DI		12	Disable Interrupt	

REGISTER CONTROL INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
SIO		6	Start (Trigger) Serial I/O	
STM		6	Start Timer	

INPUT/OUTPUT INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
PEX		15	$PE_{15-8} \leftarrow B, PE_{7-0} \leftarrow C$	
PER		12	Port E AB Mode	

(Note)

The clock cycles shown here are indicated about in care of that the program are located in the on-chip ROM, and the other data are located in the on-chip RAM or external memory requiring no wait. If the programs were located in the on-chip RAM or external memory, then the clock cycles are shortened by two clock cycles per one-byte fetch.

Ex. PER instruction (2-byte instruction)

In case of the on-chip ROM access: 12 clock cycles

In case of the on-chip RAM or external memory access: 12– (2x2) = 8 clock cycles

1 clock cycle = 4/fosz

ELECTRICAL SPECIFICATIONS AND PACKAGE OUTLINES FOR μPD78C05A/μPD78C06A

for extended temperature range
T_a = −40 to +85°C

μPD78C05AG ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNITS
Supply Voltage	V_{CC}		−0.3 to +7.0	V
Input Voltage	V_I		−0.3 to V_{CC} + 0.3	V
Output Voltage	V_O		−0.3 to V_{CC} + 0.3	V
Output High Current	I_{OH}	Device Total	−5	mA
Output Low Current	I_{OL}	Device Total	43.5	mA
Operating Temperature	T_{opt}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

DC CHARACTERISTICS

(T_a = −40 to +85°C, V_{CC} = +5.0V ± 10%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH1}	INT_{0-1}, $\overline{WAIT}$, PB_{0-7}, PC_{0-5}	0.7 V_{CC}		V_{CC}	V
	V_{IH2}	$\overline{RESET}$, $\overline{SCK}$, REL, SI	0.75 V_{CC}		V_{CC}	V
	V_{IH3}	DB_{0-7}	V_{CC} −2.0		V_{CC}	V
	V_{IH4}	X1	V_{CC} −0.5		V_{CC}	V
Input Low Voltage	V_{IL1}	INT_{0-1}, $\overline{WAIT}$, PB_{0-7}, PC_{0-5}	0		0.3 V_{CC}	V
	V_{IL2}	$\overline{RESET}$, $\overline{SCK}$, REL, SI	0		0.25 V_{CC}	V
	V_{IL3}	DB_{0-7}	0		0.8	V
	V_{IL4}	X1	0		0.5	V
Output High Voltage	V_{OH1}	I_{OH} = −100 μA	2.4			V
	V_{OH2}	I_{OH} = −50 μA	V_{CC} −0.5			V
Output Low Voltage	V_{OL}	I_{OL} = 1.8 mA			0.45	V
Input High Current	I_{IH1}	V_{IN} = V_{CC} (REL)	7		100	μA
	I_{IH2}	V_{IN} = V_{CC} (X1)			45	μA
Input Low Current	I_{IL1}	V_{IN} = 0V ($\overline{WAIT}$, PC_{0-5})	−7		−100	μA
	I_{IL2}	V_{IN} = 0V (X1)			−45	μA
Input High Leakage Current	I_{LIH}	V_{IN} = V_{CC} (Except REL, X1)			3.2	μA
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0V (Except $\overline{WAIT}$, PC_{0-5}, X1)			−3.2	μA
	I_{LIL2}	V_{IN} = 0V (STOP Mode, X1)			−3.2	μA
Output High Leakage Current	I_{LOH}	V_{OUT} = V_{CC}			3.2	μA
Output Low Leakage Current	I_{LOL}	V_{OUT} = 0V			−3.2	μA
V_{CC} Supply Current	I_{CC1}	Operation Mode		4.0	7.5	mA
	I_{CC2}	HALT Mode		1.2	2.7	mA
	I_{CC3}	STOP Mode (X1 = 0V, X2 = Open)		1	20	μA

CAPACITANCE

(T_a = 25°C, V_{CC} = GND = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_C = 1MHz			15	pF
Output Capacitance	C_O	Unmeasured Pins returned to 0V			15	pF
I/O Capacitance	$C_{I/O}$				15	pF

AC CHARACTERISTICS CLOCK TIMING

(T_a = −40 to +85°C, V_{CC} = +5.0V ± 10 %)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
X1 Input Cycle Time	t_{CYX}		160		10000	ns
X1 Input Low Time	t_{XXL}		75			ns
X1 Input High Time	t_{XXH}		75			ns
ϕ_{OUT} Cycle Time	$t_{CY\phi}$		640		40000	ns
ϕ_{OUT} Low Time	$t_{\phi\phi L}$		195			ns
ϕ_{OUT} High Time	$t_{\phi\phi H}$		195			ns
ϕ_{OUT} Rise/Fall Time	t_r, t_f				120	ns

READ/WRITE OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RD}$ L. E. to ϕ_{OUT} L. E.	$t_{R\phi}$	$t_{CY\phi}$ = 660 ns	180			ns
Address (PE_{0-15}) to Data Input	t_{AD1}				790 +660xN	ns
$\overline{RD}$ T. E. to Address	t_{RA}		180(T3) 840(T4)			ns
$\overline{RD}$ L. E. to Data Input	t_{RD}				460 +660xN	ns
$\overline{RD}$ T. E. to Data Hold Time	t_{RDH}		0			ns
$\overline{RD}$ Low Time	t_{RR}		1070 +660xN			ns
$\overline{RD}$ L. E. to $\overline{WAIT}$ L. E.	t_{RWT}				460	ns
Address (PE_{0-15}) to $\overline{WAIT}$ L. E.	t_{AWT1}				790	ns
$\overline{WAIT}$ Set Up Time to ϕ_{OUT} L. E.	t_{WTS}		370			ns
$\overline{WAIT}$ Hold Time after ϕ_{OUT} L. E.	t_{WTH}		0			ns
M1 to RD L. E.	t_{MR}		108			ns
RD T. E. to M1	t_{RM}		130			ns
ϕ_{OUT} L. E. to $\overline{WR}$ L. E.	$t_{\phi W}$				175	ns
Address (PE_{0-15}) to ϕ_{OUT} T. E.	$t_{A\phi}$		90			ns
Address (PE_{0-15}) to Data Output	t_{AD2}		510			ns
Data Output to $\overline{WR}$ T. E.	t_{DW}		740 +660xN			ns
$\overline{WR}$ T. E. to Data Stable Time	t_{WD}		130			ns
Address (PE_{0-15}) to $\overline{WR}$ L. E.	t_{AW}		460			ns
$\overline{WR}$ T. E. to Address Stable Time	t_{WA}		180			ns
$\overline{WR}$ Low Time	t_{WW}		690 +660xN			ns
$\overline{WR}$ L. E. to $\overline{WAIT}$ L. E.	t_{WWT}				110	ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	1270			ns
		$\overline{SCK}$ Output	1280		80000	ns
$\overline{SCK}$ Low Time	t_{KKL}	$\overline{SCK}$ Input	515			ns
		$\overline{SCK}$ Output	520			ns
$\overline{SCK}$ High Time	t_{KKH}	$\overline{SCK}$ Input	515			ns
		$\overline{SCK}$ Output	520			ns
SI Set Up Time to $\overline{SCK}$ T. E.	t_{SIS}		200			ns
SI Hold Time after $\overline{SCK}$ T. E.	t_{SIH}		250			ns
$\overline{SCK}$ L. E. to SO Delay Time	t_{KO}				300	ns

Note: 1) Input timings are measured at V_{IHMIN} and V_{ILMAX}.

2) Output timings are measured at V_{OH} = 2.4 V and V_{OL} = 0.45 V with 1TTL + 200 pF load.

3) L. E. = Leading Edge, T. E. = Trailing Edge

4) N is number of T_{WAIT}.

BUS TIMING DEPENDING ON tCYC

(T_a = −40 to + 85°C)

SYMBOL	CALCULATING EXPRESSION	MIN/MAX	UNITS
$t_{R\phi}$	(1/2)T − 150	MIN	ns
t_{AD1}	(3/2+N)T − 200	MAX	ns
$t_{RA(T3)}$	(1/2)T − 150	MIN	ns
$t_{RA(T4)}$	(3/2)T − 150	MIN	ns
t_{RD}	(1+N)T − 200	MAX	ns
t_{RR}	(2+N)T − 250	MIN	ns
t_{RWT}	T − 200	MAX	ns
t_{AWT1}	(3/2)T − 200	MAX	ns
t_{WTS}	(1/3)T + 150	MIN	ns
t_{MR}	(3/8)T − 140	MIN	ns
t_{RM}	(1/2)T − 200	MIN	ns
$t_{A\phi}$	(1/2)T − 240	MIN	ns
t_{AD2}	T − 150	MIN	ns
t_{DW}	(3/2+N)T − 250	MIN	ns
t_{WD}	(1/2)T − 200	MIN	ns
t_{AW}	T − 200	MIN	ns
t_{WA}	(1/2)T − 150	MIN	ns
t_{WW}	(3/2+N)T − 300	MIN	ns
t_{WWT}	(1/2)T − 220	MAX	ns
t_{CYK}	2T	MIN	ns
t_{KKL}	T − 120	MIN	ns
t_{KKH}	T − 120	MIN	ns

Note: 1) N = Number of T_{WAIT}.

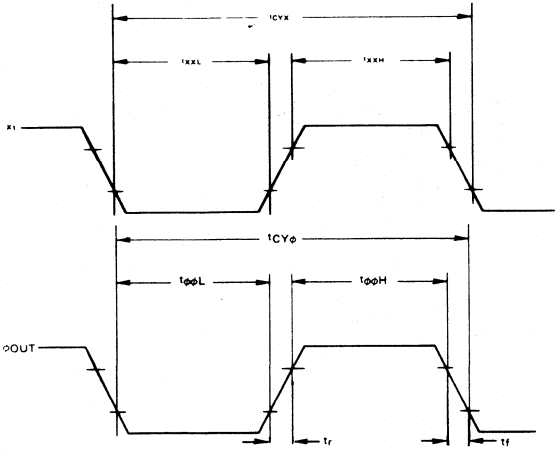
2) T = $T_{CY\phi}$.

3) t_{CY} assumes 50 % duty cycle on X1.

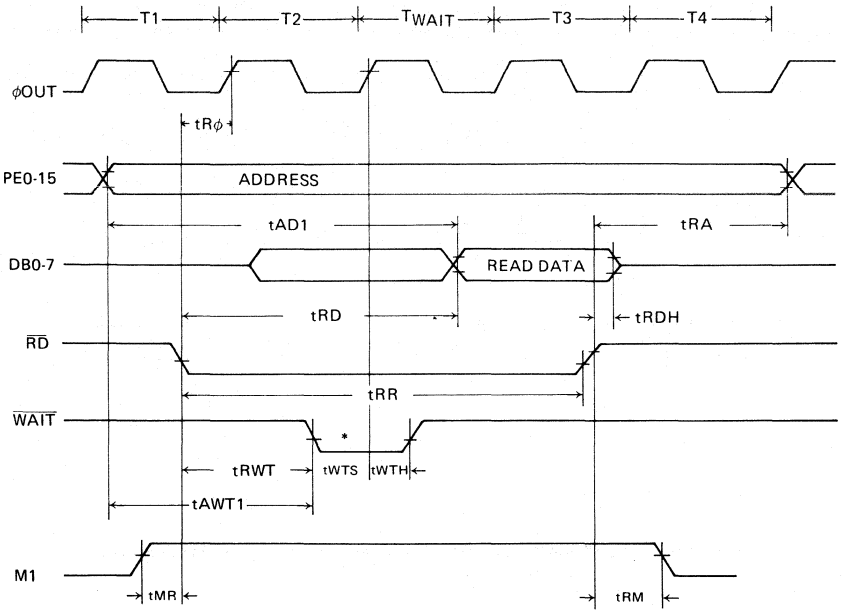
4) The items out of this table are not dependent on t_{CY}.

TIMING WAVEFORMS

CLOCK TIMING

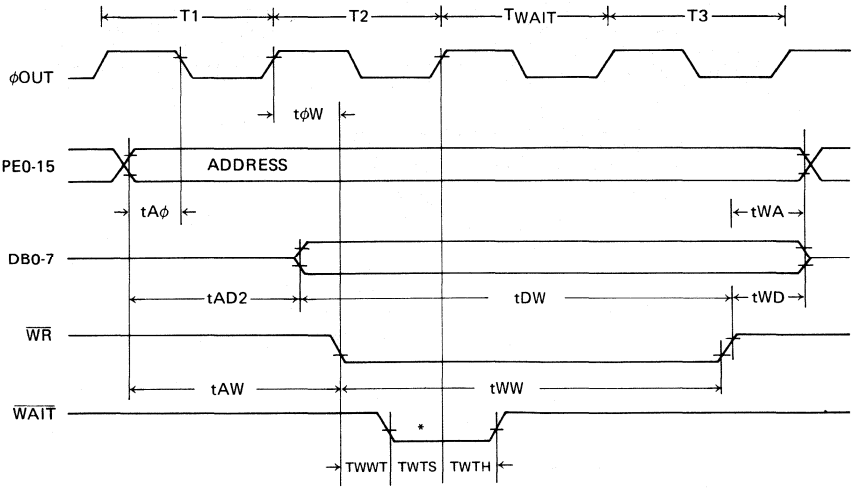


READ OPERATION



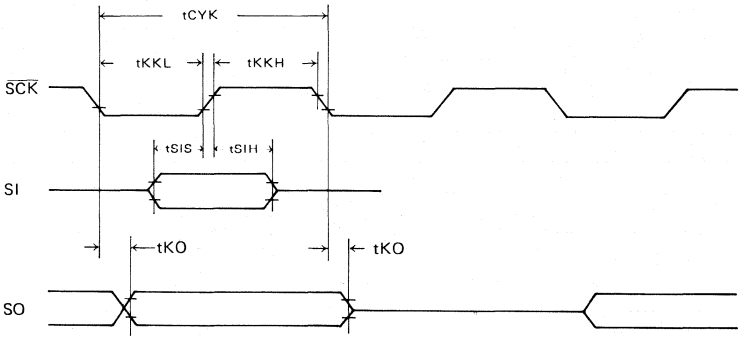
* WAIT signal must be remained stable during t_{WTS} and t_{WTH}.
If it is unstable, misoperation may occur.

WRITE OPERATION



* WAIT signal must be remained stable during t_{WTS} and t_{WTH}.
If it is unstable, misoperation may occur.

SERIAL OPERATION



Low Power Data Memory Retention Characteristics for STOP Mode Operation

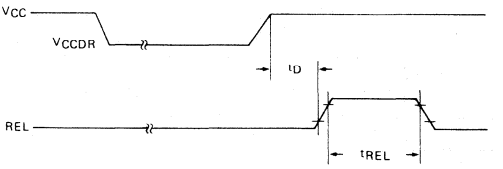
(T_a = −40 to +85°C)

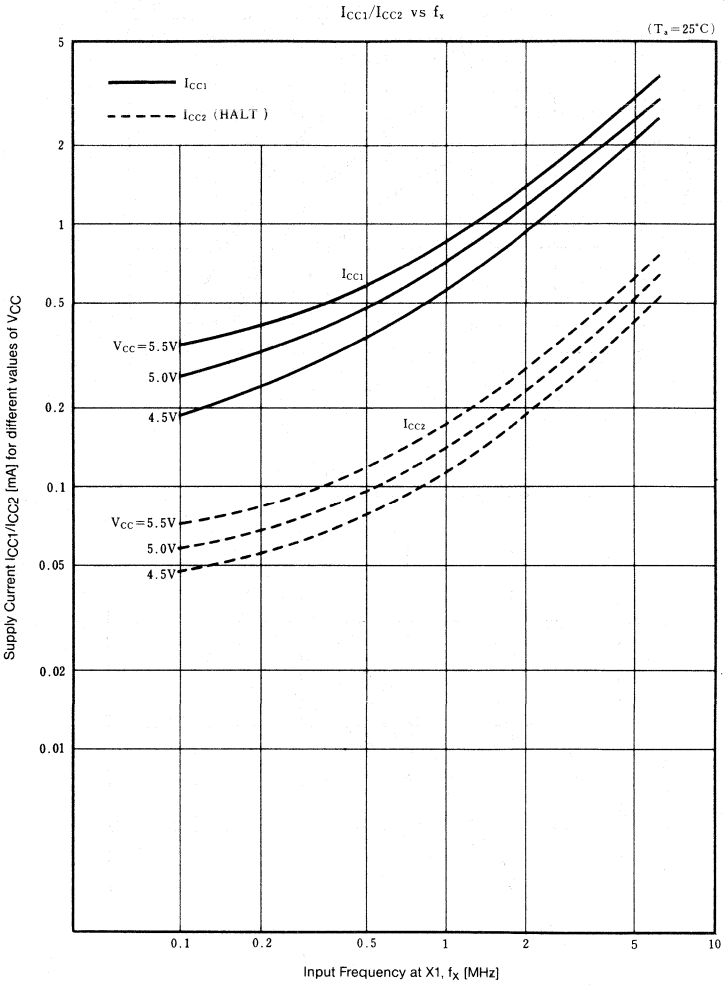
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Voltage	V_{CCDR}		2.0			V
Data Retention Supply Current	I_{CCDR}	V_{CCDR} = 2.0V, X1 = 0V, X2 = Open		0.8	20	μA
Data Retention Input Low REL Voltage	V_{ILDR}		0		0.2 V_{CCDR}	V
Data Retention Input High $\overline{RESET}$ Voltage	V_{IHDR}		0.8 V_{CCDR}		V_{CCDR}	V
REL Input Delay Time	t_D		500			μs
REL Input High Time	t_{REL}		10			μs

Note: In data retention mode,

1) Input voltages to $\overline{WAIT}$ and PC_{0-5} pins (with pull-up resisters) should be maintained same as V_{CCDR} level,

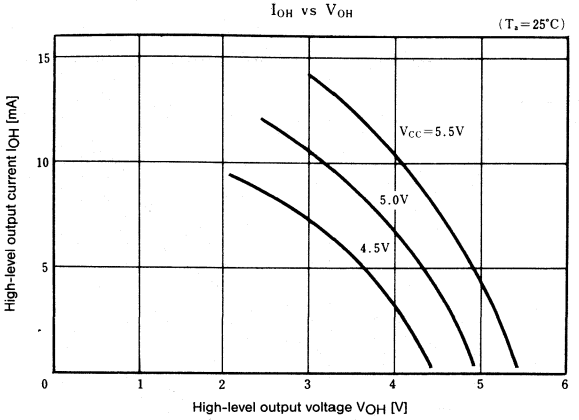
2) Other input voltages should be kept less than V_{CCDR} level.




I_{CC1}/I_{CC2} vs f_x
(T_a=25°C)
I_{CC1}
I_{CC2} (HALT)
I_{CC1}
V_{CC}=5.5V
5.0V
4.5V
I_{CC2}
V_{CC}=5.5V
5.0V
4.5V
Supply Current I_{CC1}/I_{CC2} [mA] for different values of V_{CC}
5
2
1
0.5
0.2
0.1
0.05
0.02
0.01
0.1
0.2
0.5
1
2
5
10
Input Frequency at X1, f_X [MHz]

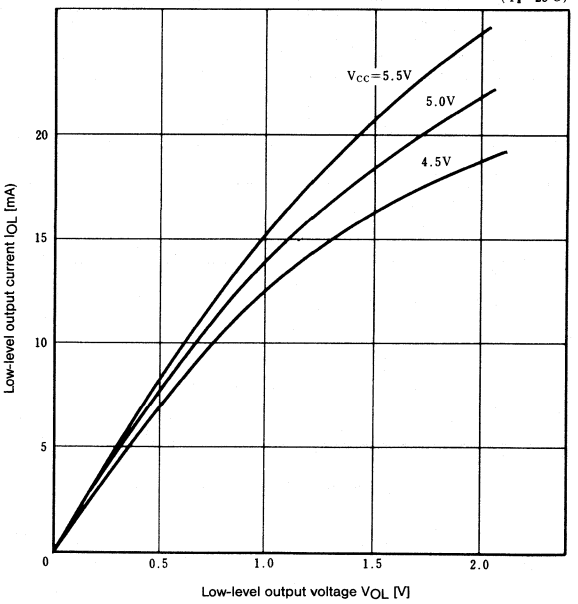
I_{OH} vs V_{OH}

(T_a=25°C)



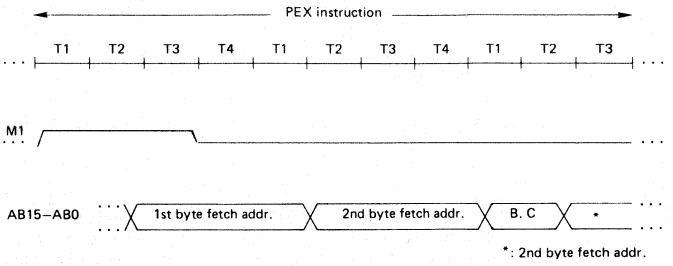
I_{OL} vs V_{OL}

(T_a=25°C)



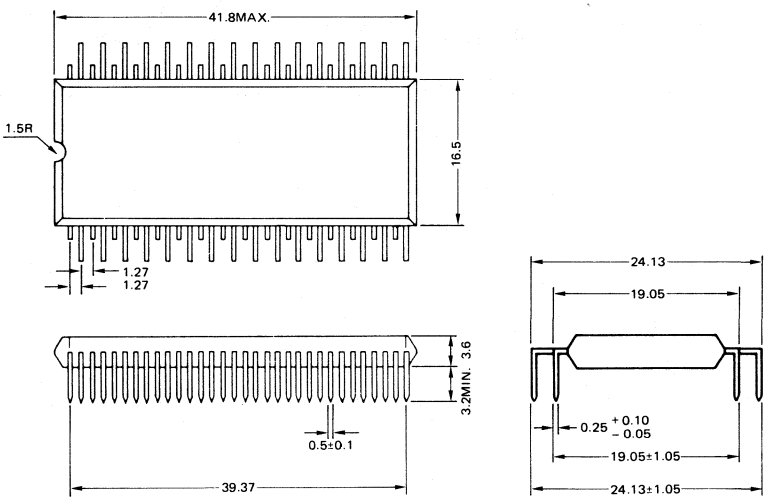
PORT E OPERATION μPD78C05A

The following diagram is the timing at PEX instruction execution.



*: 2nd byte fetch addr.

64 PIN PLASTIC QUIP OUTLINE (Unit : mm) for μPD78C05AG



Differences between μPD78C06A and μPD78C05A

Parameter		μPD78C06A	μPD78C05A
4K-byte built-in ROM		Yes	No
Internal WAIT of built-in ROM		2 WAIT cycle	No
Port E (Address bus)	After reset	Port mode	Address bus mode
	Latch function	Yes	No
	PEX instruction	PE15 – 8⇦B and PE7 – 0⇦C are executed and latched at M3T1 timing. Output is unchanged until the next PEX or PER instruction is executed.	AB15 – 8⇦B and AB7 – 0⇦C are executed only at M3T1 timing and the contents of the internal address bus are output at the other timing.
$\overline{RD}$/$\overline{WR}$ signal		Output against the address space of 1000H – FF7FH (4096 – 65407).	Output against the address space of 000H – FF7FH (0 – 65407).
M1 output		No	Yes
Pin connection		Difference	
Package		64 pin Flat 64 pin QUIP	64 pin QUIP

μPD78C06AG ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNITS
Supply Voltage	V_{CC}		−0.3 to +7.0	V
Input Voltage	V_I		−0.3 to V_{CC} + 0.3	V
Output Voltage	V_O		−0.3 to V_{CC} + 0.3	V
Output High Current	I_{OH}	Device Total	−5	mA
Output Low Current	I_{OL}	Device Total	45	mA
Operating Temperature	T_{opt}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

DC CHARACTERISTICS

(T_a = −40 to +85°C, V_{CC} = +5.0V ± 10%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH1}	INT_{0-1}, $\overline{WAIT}$, PB_{0-7}, PC_{0-5}	0.7 V_{CC}		V_{CC}	V
	V_{IH2}	$\overline{RESET}$, $\overline{SCK}$, REL, SI	0.75 V_{CC}		V_{CC}	V
	V_{IH3}	DB_{0-7}	V_{CC} −2.0		V_{CC}	V
	V_{IH4}	X1	V_{CC} −0.5		V_{CC}	V
Input Low Voltage	V_{IL1}	INT_{0-1}, $\overline{WAIT}$, PB_{0-7}, PC_{0-5}	0		0.3 V_{CC}	V
	V_{IL2}	$\overline{RESET}$, $\overline{SCK}$, REL, SI			0.25 V_{CC}	V
	V_{IL3}	DB_{0-7}	0		0.8	V
	V_{IL4}	X1	0		0.5	V
Output High Voltage	V_{OH1}	I_{OH} = −100 μA	2.4			V
	V_{OH2}	I_{OH} = −50 μA	V_{CC} −0.5			V
Output Low Voltage	V_{OL}	I_{OL} = 1.8 mA			0.45	V
Input High Current	I_{IH1}	V_{IN} = V_{CC} (REL)	7		100	μA
	I_{IH2}	V_{IN} = V_{CC} (X1)			45	μA
Input Low Current	I_{IL1}	V_{IN} = 0V ($\overline{WAIT}$, PC_{0-5})	−7		−100	μA
	I_{IL2}	V_{IN} = 0V (X1)			−45	μA
Input High Leakage Current	I_{LIH}	V_{IN} = V_{CC} (Except REL, X1)			3.2	μA
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0V (Except $\overline{WAIT}$, PC_{0-5}, X1)			−3.2	μA
	I_{LIL2}	V_{IN} = 0V (STOP Mode, X1)			−3.2	μA
Output High Leakage Current	I_{LOH}	V_{OUT} = V_{CC}			3.2	μA
Output Low Leakage Current	I_{LOL}	V_{OUT} = 0V			−3.2	μA
V_{CC} Supply Current	I_{CC1}	Operation Mode		4.0	7.5	mA
	I_{CC2}	HALT Mode		1.2	2.7	mA
	I_{CC3}	STOP Mode (X1 = 0V, X2 = Open)		1	20	μA

DC CHARACTERISTICS

(T_a = −40 to +85°C, V_{CC} = +2.5V to +6.0V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Voltage High	V_{IH1}	Except DB_{0-7}, X1		0.8 V_{CC}		V_{CC}	V
	V_{IH2}	DB_{0-7}		0.7 V_{CC}		V_{CC}	V
	V_{IH3}	X1	(1)	0.9 V_{CC}		V_{CC}	V
			(2)	V_{CC} −0.5		V_{CC}	V
Input Voltage Low	V_{IL1}	Except DB_{0-7}, X1		0		0.2 V_{CC}	V
	V_{IL2}	DB_{0-7}	(1)	0		0.18 V_{CC}	V
			(2)	0		0.8	V
	V_{IL3}	X1	(1)	0		0.1 V_{CC}	V
			(2)	0		0.5	V
Output Voltage	V_{OH}	I_{OH} = −50μA		V_{CC} −0.5			V
Output Voltage Low	V_{OL}	I_{OL} = 400μA				0.45	V
Input Current High	I_{IH1}	V_{IN} = V_{CC} (REL)		2.5		110	μA
	I_{IH2}	V_{IN} = V_{CC} (X1)				50	μA
Input Current Low	I_{IL1}	V_{IN} = 0V ($\overline{WAIT}$, PC_{0-5})		−2.5		−110	μA
	I_{IL2}	V_{IN} = 0V (X1)				−50	μA
Input Leakage Current High	I_{LIH}	V_{IN} = V_{CC} (Except REL, X1)				3.5	μA
Input Leakage Current Low	I_{LIL1}	V_{IN} = 0V (Except $\overline{WAIT}$, PC_{0-5}, X1)				−3.5	μA
	I_{LIL2}	V_{IN} = 0V (STOP Mode, X1)				−3.5	μA
Output Leakage Current High	I_{LOH}	V_{OUT} = V_{CC}				3.5	μA
Output Leakage Current Low	I_{LOL}	V_{OUT} = 0V				−3.5	μA
V_{CC} Supply Current	I_{CC1}	Operation Mode	V_{CC} = 3V, $t_{CY\phi}$ = 8μs		0.7	1.5	mA
			V_{CC} = 6V, $t_{CY\phi}$ = 1.32μs		5.0	9.0	mA
	I_{CC2}	HALT Mode	V_{CC} = 3V, $t_{CY\phi}$ = 8μs		0.2	0.5	mA
			V_{CC} = 6V, $t_{CY\phi}$ = 1.32μs		1.5	3.0	mA
	I_{CC3}	STOP Mode	(X1 = 0V, X2 = Open)		1.	20	μA

Notes 1: 2.5V ≦ V_{CC} ≦ 4.5V
2: 4.5V ≦ V_{CC} ≦ 6.0V

CAPACITANCE

(T_a = 25°C, V_{CC} = GND = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_C = 1MHz			15	pF
Output Capacitance	C_O	Unmeasured Pins returned to 0V			15	pF
I/O Capacitance	$C_{I/O}$				15	pF

AC CHARACTERISTICS CLOCK TIMING:

(T_a = −40°C to +85°C)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} = 5.0V ± 10% MIN	MAX	UNIT	V_{CC} = 2.5V to +6.0V MIN	MAX	UNIT
X1 Input Cycle Time	t_{CYX}			160	10000	ns	1.65	10	μs
X1 Input Low Level Width	t_{XXL}			75		ns	0.78		μs
X1 Input High Level Width	t_{XXH}			75		ns	0.78		μs
$Ø_{OUT}$ Cycle Time	$t_{CYØ}$			1280	80000	ns	13.2	80	μs
$Ø_{OUT}$ Low Level Width	$t_{ØØL}$			515		ns	6.35		μs
$Ø_{OUT}$ High Level Width	$t_{ØØH}$			515		ns	6.35		μs
$Ø_{OUT}$ Rise/Fall Time	t_r, t_f				120	ns		250	ns
Clock Oscillation Frequency (X1, X2)	f_{OSC}	Crystal oscillation	4.5V ≦ V_{CC} ≦ 6.0V				3.5	6.25	MHz
		Ceramic oscillation	4.5V ≦ V_{CC} ≦ 6.0V				0.1	6.25	MHz
			V_{CC} = 3.5V				0.1	4.0	MHz
			V_{CC} = 2.7V				0.1	0.6	MHz

READ/WRITE OPERATION

(T_a = −40°C to +85°C)

PARAMETER	SYMBOL	V_{CC} = +5.0V ± 10% TEST CONDITIONS	MIN	MAX	UNIT	V_{CC} = 2.5V to +6.0V TEST CONDITIONS	MIN	MAX	UNIT
$\overline{RD}$ L.E. to $Ø_{OUT}$ L.E.	$t_{RØ}$		180		ns		3.1		μs
Address (PE_{0-15}) to Data Input	t_{AD1}			790 +660xN	ns			9.7 +6.6xN	μs
$\overline{RD}$ T.E. to Address	t_{RA}		180(T3) 840(T4)		ns		3.05(T3) 9.65(T4)		μs
$\overline{RD}$ L.E. to Data Input	t_{RD}			460 +660xN	ns			6.4 +6.6xN	μs
$\overline{RD}$ T.E. to Data Hold Time	t_{RDH}		0		ns		0		μs
$\overline{RD}$ Low Level Width	t_{RR}		1070 +660xN		ns		12.93 +6.6xN		μs
$\overline{RD}$ L.E. to $\overline{WAIT}$ L.E.	t_{RWT}			460	ns			6.4	μs
Address (PE_{0-15}) to $\overline{WAIT}$ L.E.	t_{AWT1}			790	ns			9.7	μs
$\overline{WAIT}$ Set Up Time to $Ø_{OUT}$ L.E.	t_{WTS}		370		ns		2.35		μs
$\overline{WAIT}$ Hold Time after $Ø_{OUT}$ L.E.	t_{WTH}	$t_{CYØ}$ = 1320ns	0		ns	$t_{CYØ}$ = 13.2μs	0		μs
$Ø_{OUT}$ L.E. to $\overline{WR}$ L.E.	$t_{ØW}$			175	ns			0.25	μs
Address (PE_{0-15}) to $Ø_{OUT}$ T.E.	$t_{AØ}$		420		ns		6.1		μs
Address (PE_{0-15}) to Data Output	t_{AD2}		510		ns		6.4		μs
Data Output to $\overline{WR}$ T.E.	t_{DW}		740 +660xN		ns		9.35 +6.6xN		μs
$\overline{WR}$ T.E. to Data Stable Time	t_{WD}		130		ns		3.05		μs
Address (PE_{0-15}) to $\overline{WR}$ L.E.	t_{AW}		460		ns		6.35		μs
$\overline{WR}$ T.E. to Address Stable Time	t_{WA}		180		ns		3.05		μs
$\overline{WR}$ Low Level Width	t_{WW}		690 +660xN		ns		9.5 +6.6xN		μs
$\overline{WR}$ L.E. to $\overline{WAIT}$ L.E.	t_{WWT}			110	ns			3.08	μs

N: Number of T_{WAIT}

SERIAL OPERATION

(T_a = −40°C to +85°C)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} = +5.0V ± 10% MIN	MAX	UNIT	V_{CC} = +2.5V to + 6.0V MIN	MAX	UNIT
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	1270		ns	13.2		μs
		$\overline{SCK}$ Output	1280	80000	ns	13.2	80	μs
$\overline{SCK}$ Low Level Width	t_{KKL}	$\overline{SCK}$ Input	515		ns	6.35		μs
		$\overline{SCK}$ Output	520		ns	6.35		μs
$\overline{SCK}$ High Level Width	t_{KKH}	$\overline{SCK}$ Input	515		ns	6.35		μs
		$\overline{SCK}$ Output	520		ns	6.35		μs
SI Set Up Time to $\overline{SCK}$ T.E.	t_{SIS}		200		ns	0.3		μs
SI Hold Time after $\overline{SCK}$ T.E.	t_{SIH}		250		ns	0.5		μs
$\overline{SCK}$ L.E. to SO Delay Time	t_{KO}			300	ns		0.8	μs

Notes 1: Input timings are measured at V_{IHMIN} and V_{ILMAX}

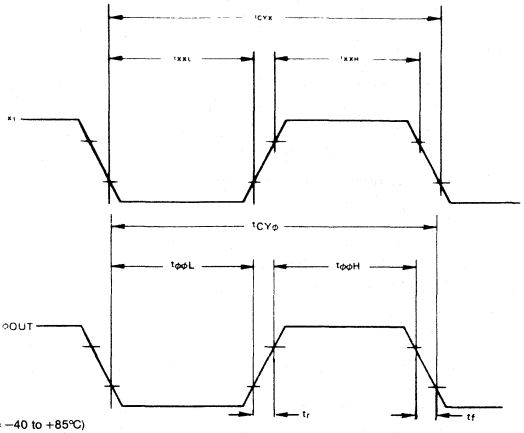
2: Output timings are measured at with 1TTL + 200pF load. V_{OH} = 2.4V and V_{OL} = 0.45V (V_{CC} = 5.0V ± 10%) V_{OH} = 0.7V_{CC} and V_{OL} = 0.3V_{CC} (V_{CC} = 2.5V to +6.0V)

3: L.E. = Leading Edge, T.E. = Trailing Edge

4: Use the following table (on same page) to calculate AC parameters in $t_{CYØ}$ 1320ns (V_{CC} = 5.0V ± 10%) resp. $t_{CYØ}$ 13.2 μs (V_{CC} = 2.5V to + 6.0V)

TIMING WAVEFORMS

CLOCK TIMING



BUS TIMING DEPENDING ON $t_{CYØ}$

(T_a = −40 to +85°C)

SYMBOL	V_{CC} = +5.0V ± 10% CALCULATING EXPRESSION	MIN/MAX	UNIT	V_{CC} = +2.5V to +6.0V CALCULATING EXPRESSION	MIN/MAX	UNIT
$t_{RØ}$	(1/2)T − 150	MIN	ns	(1/2)T − 200	MIN	ns
t_{AD1}	(3/2+N)T − 200	MAX	ns	(3/2+N)T − 200	MAX	ns
$t_{RA(T3)}$	(1/2)T − 150	MIN	ns	(1/2)T − 250	MIN	ns
$t_{RA(T4)}$	(3/2)T − 150	MIN	ns	(3/2)T − 250	MIN	ns
t_{RD}	(1+N)T − 200	MAX	ns	(1+N)T − 200	MAX	ns
t_{RR}	(2+N)T − 250	MIN	ns	(2+N)T − 270	MIN	ns
t_{RWT}	T − 200	MAX	ns	T − 200	MAX	ns
t_{AWT1}	(3/2)T + 200	MAX	ns	(3/2)T − 200	MAX	ns
t_{WTS}	(1/3)T + 150	MIN	ns	(1/3)T + 150	MIN	ns
$t_{AØ}$	T − 240	MIN	ns	T − 500	MIN	ns
t_{AD2}	T − 150	MIN	ns	T − 200	MIN	ns
t_{DW}	(3/2+N)T − 250	MIN	ns	(3/2+N)T − 550	MIN	ns
t_{WD}	(1/2)T − 200	MIN	ns	(1/2)T − 250	MIN	ns
t_{AW}	T − 200	MIN	ns	T − 250	MIN	ns
t_{WA}	(1/2)T − 150	MIN	ns	(1/2)T − 250	MIN	ns
t_{WW}	(3/2+N)T − 300	MIN	ns	(3/2+N)T − 400	MIN	ns
t_{WWT}	(1/2)T − 220	MAX	ns	(1/2)T − 220	MAX	ns
t_{CYK}	2T	MIN	ns	2T	MIN	ns
t_{KKL}	T − 120	MIN	ns	T − 250	MIN	ns
t_{KKH}	T − 120	MIN	ns	T − 250	MIN	ns

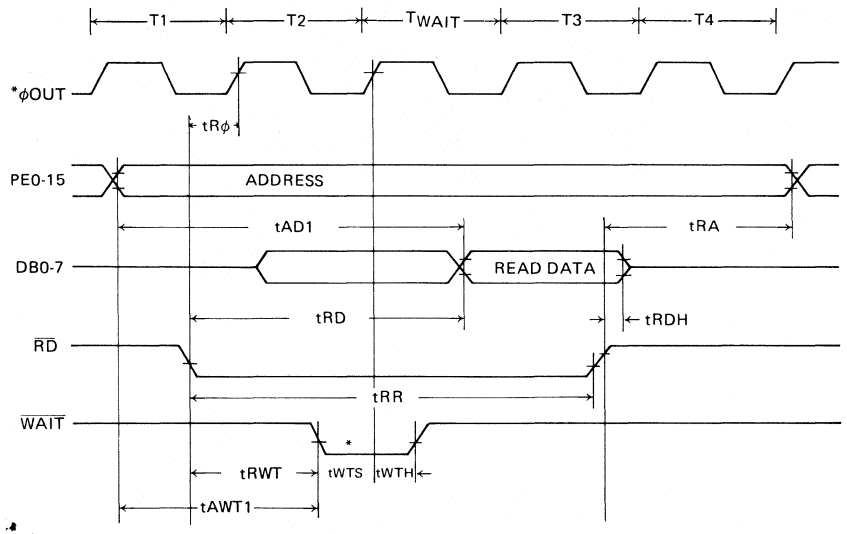
Notes 1. N = Number of T_{WAIT}

2. T = $t_{CYØ}$/2

3. For external clock, 50% duty cycle on X1 is assumed.

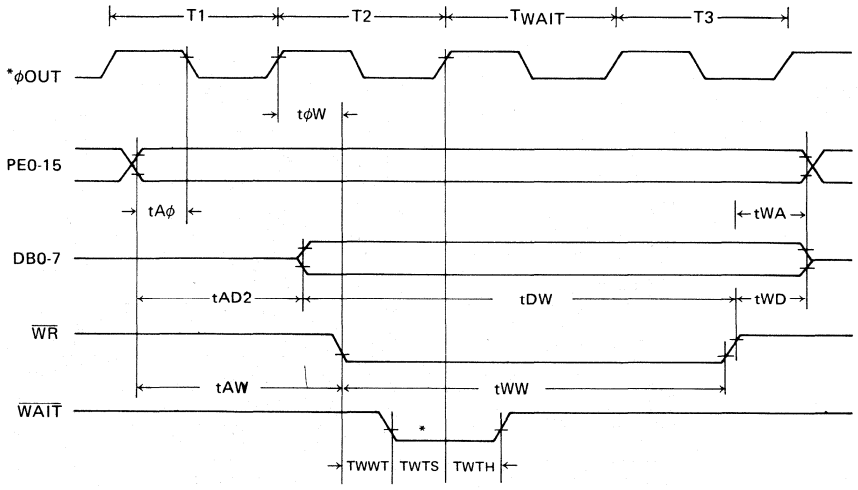
4. The items not included in this table are not dependent on $t_{CYØ}$.

READ OPERATION



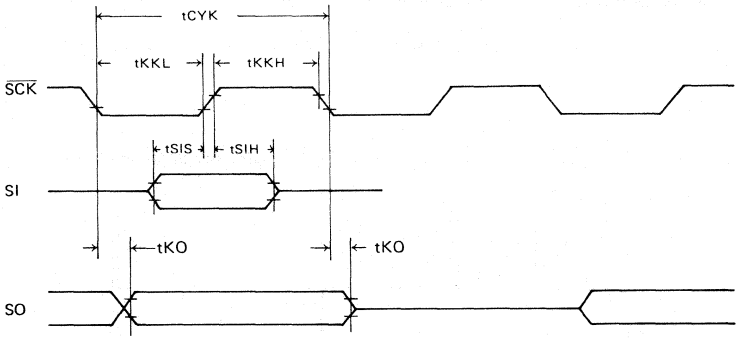
* WAIT signal must be remained stable during t_{WTS} and t_{WTH}.
If it is unstable, misoperation may occur.

WRITE OPERATION



* WAIT signal must be remained stable during t_{WTS} and t_{WTH}.
If it is unstable, misoperation may occur.

SERIAL OPERATION



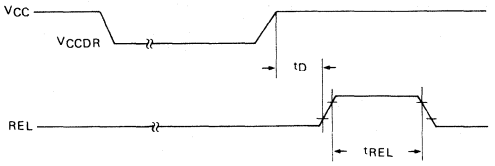
Low Power Data Memory Retention Characteristics for STOP Mode Operation

(T_a = −40 to +85°C)

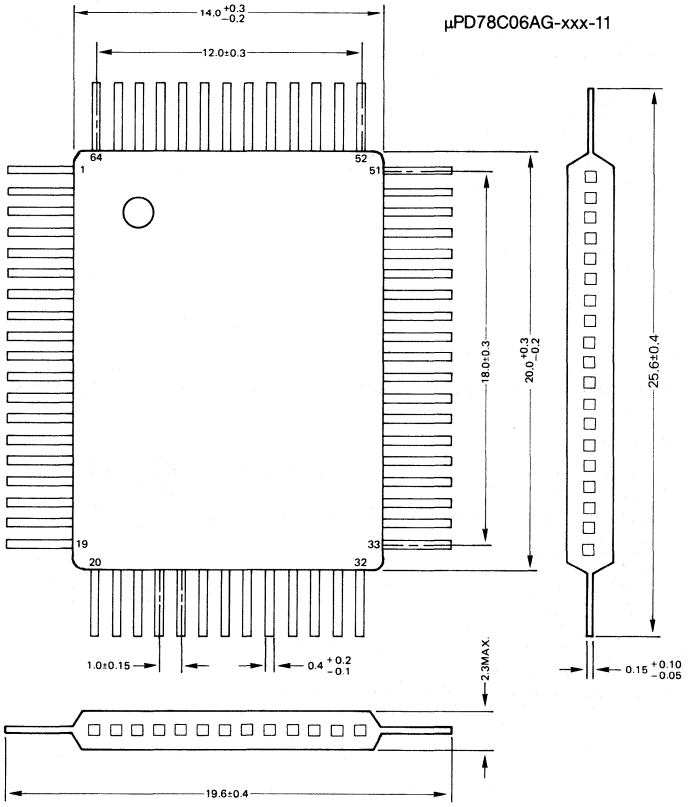
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Voltage	V_{CCDR}		2.0			V
Data Retention Supply Current	I_{CCDR}	V_{CCDR} = 2.0V, X1 = 0V, X2 = Open		0.8	20	μA
Data Retention Input Low RES Voltage	V_{ILDR}		0		0.2 V_{CCDR}	V
Data Retention Input High $\overline{RESET}$ Voltage	V_{IHDR}		0.8 V_{CCDR}		V_{CCDR}	V
REL Input Delay Time	t_D		500			μs
REL Input High Time	t_{REL}		10			μs

Note: In data retention mode,

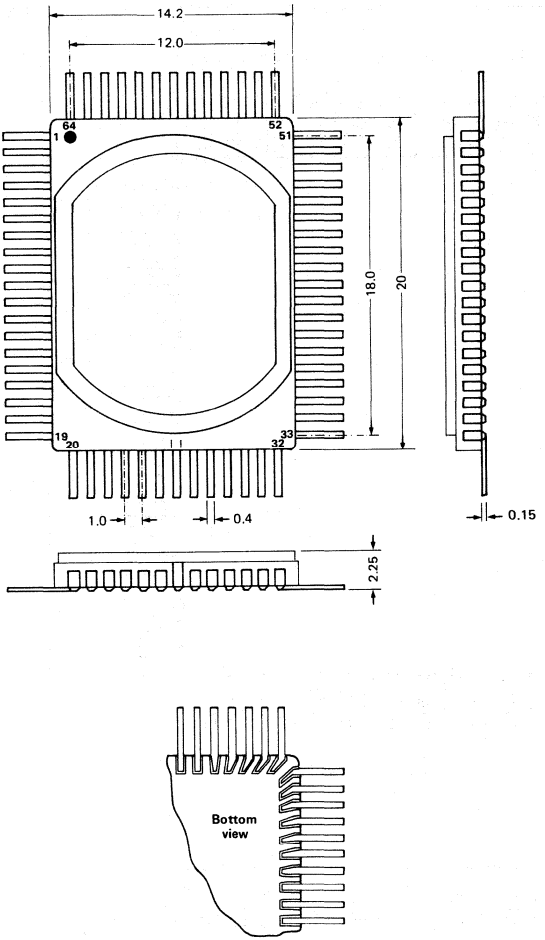
1) Input voltages to $\overline{WAIT}$ and PC_{0-5} pins (with pull-up resistors) should be maintained same as V_{CCDR} level,
2) Other input voltages should be kept less than V_{CCDR} level.



64-PIN PLASTIC FLAT PACKAGE OUTLINE, STRAIGHT LEADS (Unit : mm)
for μPD78C06AG



64-PIN CERAMIC FLAT PACKAGE OUTLINE FOR ES – REFERENCE – (Unit : mm)
for μPD78C06AG



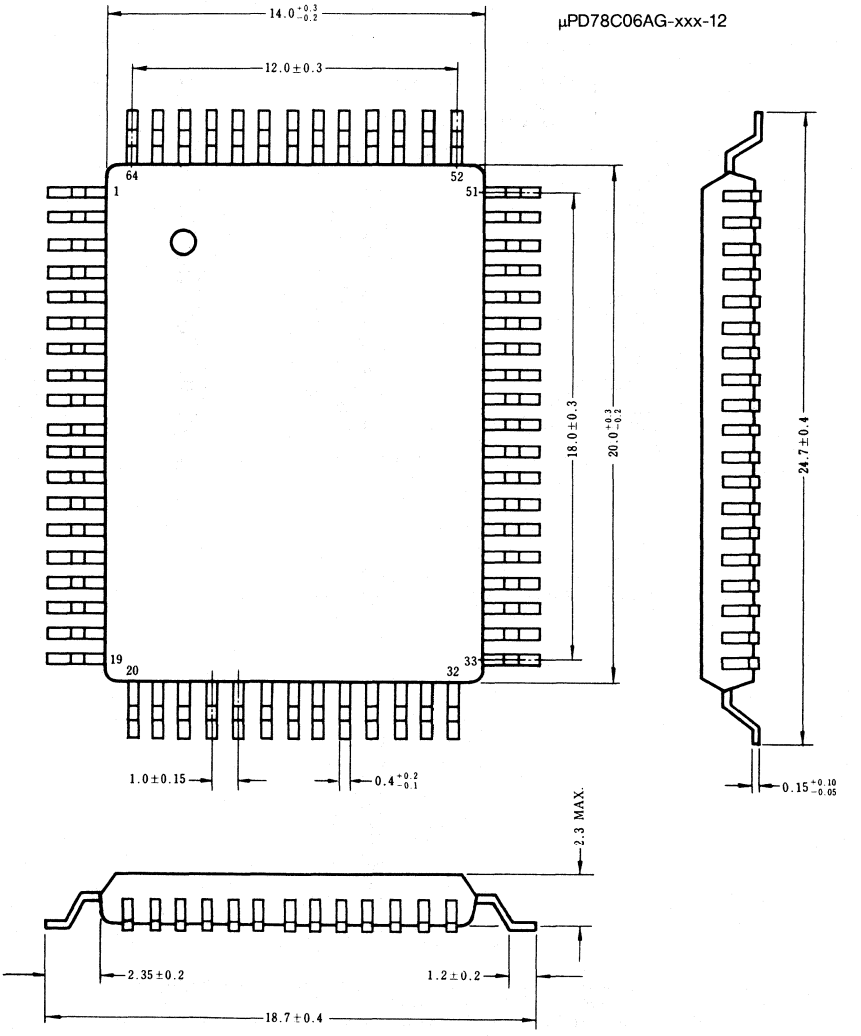
Note:

The metal cap of the device has V_{DD} (positive power supply) level because the metal cap is connected to pin No. 26 (i. e. V_{DD} pin).

The leads of the welding part at bottom of this device are formed in slant and have a chance of shorting the other lines of printed wiring board.

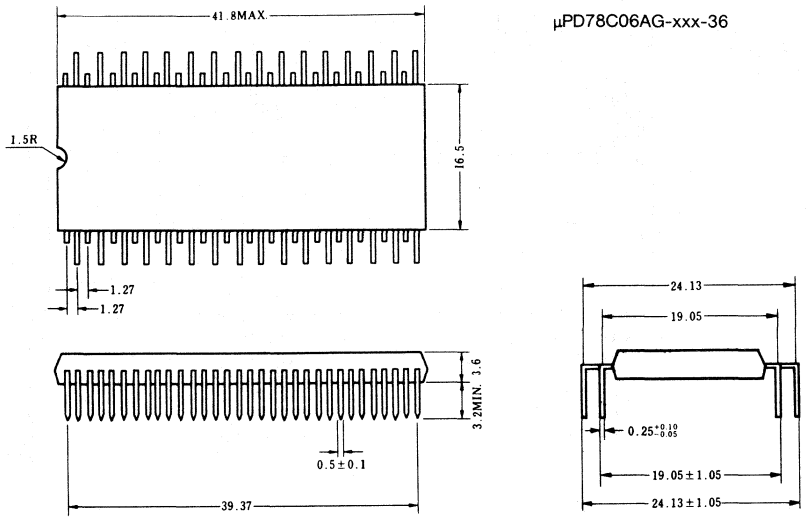
64-PIN PLASTIC FLAT PACKAGE, BENT LEADS (Unit : mm)
for μPD78C06A

μPD78C06AG-xxx-12

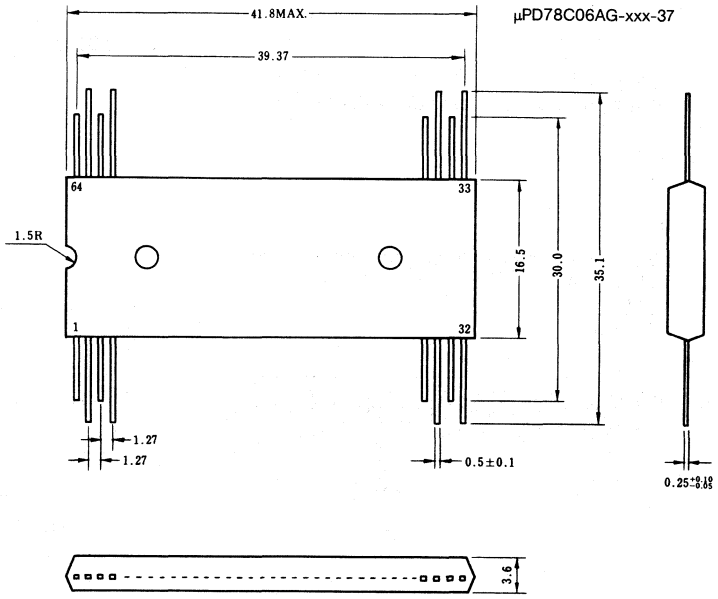


64-PIN PLASTIC QUAD-IN-LINE PACKAGE (QUIL), BENT LEADS
for μPD78C06A (Unit : mm)

μPD78C06AG-xxx-36



64-PIN PLASTIC QUAD-IN-LINE PACKAGE (QUIL) BENT LEADS (Unit : mm)
for μPD78C06AG



HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH COMPARATOR INPUTS, 8K ROM

DESCRIPTION

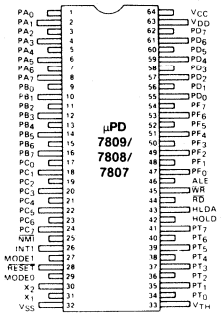
The μPD7809/7808/7807/78P09 single chip microcomputer augments the high-end in NEC's family of 8-bit microcomputers with sophisticated on-chip peripheral functionality. Like its nearest relative in the family, the μPD7811, this device has a fast internal 16-bit ALU and data paths, 256 bytes of RAM, multifunction 16-bit timer/event counter, two 8-bit timers, a USART, and two zero-cross detect inputs. Features that distinguish this device in the NEC 8-bit family are: 8K ROM, programmable threshold comparator (8 inputs), programmable WAIT function, watchdog timer, hold and hold acknowledge for DMA interface, and bit test/write instructions for both RAM and I/O.

The μPD7809 is the 8K Byte ROM version with the customers program on chip. The μPD7808 is a 4K Byte ROM version. The μPD7807 is the ROM-less version for prototyping and small volume applications. The μPD78P09 is an EPROM version of the 8K ROM μPD7809.

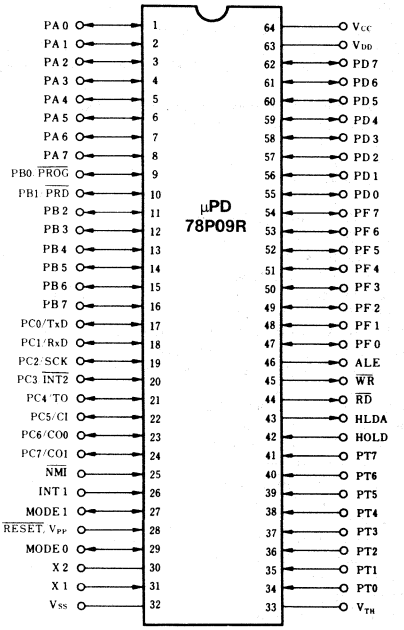
FEATURES

- NMOS silicon gate technology requiring + 5V supply
- Complete single chip microcomputer
  - 16-bit ALU
  - 8K ROM
  - 256 bytes RAM
- Large I/O capability
  - 40 I/O port lines (μPD7809/7808)
  - 24 I/O port lines (μPD7807)
  - 8 input lines
- Two zero-cross detect inputs
- Expansion capability (total of 64K memory access)
  - 8085A bus compatible
  - 56K bytes external memory address range
- Programmable threshold comparator
  - 8 inputs, 1 of 16 software selectable levels
- Full duplex USART
  - Synchronous, asynchronous and I/O mode
- 165 powerful instructions
  - 16-bit arithmetic, multiply and divide
- 1 μs instruction cycle time
- Prioritized interrupt structure
  - 3 external
  - 8 internal
- Hold, hold acknowledge for DMA interface
- Programmable WAIT function
- Watchdog timer
- Standby function
- On-chip clock generator
- 64-pin QUIL package/SDIP package

PIN CONFIGURATION



PIN CONFIGURATION μPD78P09R



PIN DESCRIPTION
μPD7809/08/07

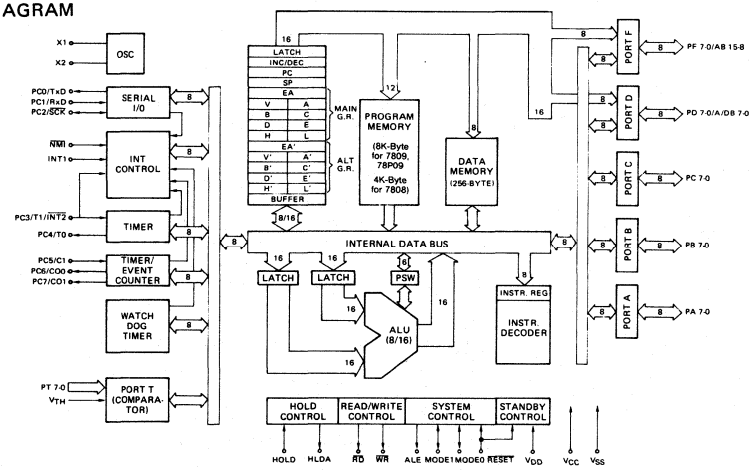
PIN NO.	PIN SYMBOL	FUNCTION	
1–8	PA_0–PA_7	Port A: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port A in input mode.	
9–16	PB_0–PB_7	Port B: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port B in input mode.	
17	PC_0	Port C: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Alternatively, Port C may be used as control lines for USART and timer counter and interrupt. Reset puts Port C in Port mode and all lines in input mode.	Transmit Data (TxD): Serial data output terminal.
18	PC_1		Receive Data (RxD): Serial data input terminal.
19	PC_2		Serial Clock (SCK): Serial clock input/output terminal. When internal clock is used, the output can be selected; when an external clock is used, the input can be selected.
20	PC_3		Timer Input ((TI)/interrupt request input (INT_2): Timer clock input terminal; can also be used as falling edge, maskable-interrupt input terminal and AC input zero-cross detection terminal.
21	PC_4		Timer Output (TO): This output signal is a square wave whose frequency is determined by the timer/counter.
22	PC_5		Counter Input (CI): External pulse input terminal to the timer/event counter.
23–24	PC_6, PC_7		Counter Outputs 0, 1 (CO_0–CO_1): Programmable rectangular wave output terminal based on timer/event counter.
25	NMI	Falling-edge, nonmaskable interrupt (NMI) input.	
26	INT_1	This signal is a rising-edge, maskable interrupt input. This input is also used to make the zero-cross detection AC input.	
27	MODE1	Used as input in conjunction with MODE0 to select appropriate memory expansion mode. Also outputs M1 Signal during each opcode fetch.	
28	RESET	(Input, active low), RESET initializes the μPD7809.	
29	MODE0	Used as input in conjunction with MODE1 to select appropriate memory expansion mode. Also used to output IO/M.	
30–31	X_2, X_1 (crystal)	This is a crystal connection terminal for system clock oscillation. When an external clock is supplied X_1 is the input.	
32	V_{SS}	Power supply ground potential.	
33	V_{TH}	V_{TH} threshold voltage input. Reference voltage for variable threshold input, Port T. Threshold voltage to each Port T input is software programmable to 16 different levels.	

PIN DESCRIPTION (cont.)

PIN NO.	PIN SYMBOL	FUNCTION
34–41	PT_1–PT_7	Eight variable threshold input ports. Ports T_0–T_7 inputs are each connected internally to comparators where the other input is the threshold voltage.
42	HOLD	HOLD request input. When high, CPU is in a HOLD state until HOLD goes low.
43	HLDA	HOLD Acknowledge output by CPU when HOLD state is accepted; goes low when HOLD is released.
44	RD	(Three-state output, active low) RD is used as a strobe to gate data from external devices onto the data bus. RD goes high during Reset.
45	WR	(Three-state output, active low) WR, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. WR goes high during Reset.
46	ALE	The strobe signal is for latching the address signal to the output from PD_7–PD_0 when accessing external expansion memory.
47–54	PF_0–PF_7	Port F: (Three-state input/output) 8-bit programmable I/O port. Each line configurable independently as an input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
55–62	PD_0–PD_7	Port D: 8-bit programmable I/O port. This byte can be designated as either input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
63	V_{DD}	This is a backup power terminal for on-chip RAM.
64	V_{CC}	+5V power supply.

Notes: 1 clock cycle = 1 CL = 3/f.
1 machine cycle = 3 or 4 clock cycles.
1 instruction cycle = 1 to 19 machine cycles.
f: System clock frequency (MHz).

BLOCK DIAGRAM



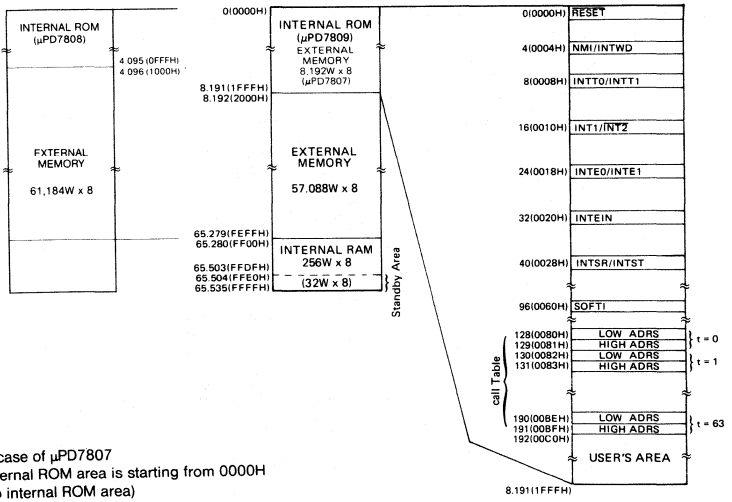
Note: The μPD7807 has no on chip ROM

INSTRUCTION SET

In addition to the basic 7800 family instruction set, the following instructions are incorporated in the μPD7809/7808/7807

- 16-bit data transfer between memory, registers, and extended accumulator
- 16-bit addition and subtraction
- 16-bit comparison and skip
- 16-bit and, or, ex-or operation
- 16-bit data shift and rotation
- Multiply
  8-bit by 8-bit, 16-bit product
  Less than 8 μs execution-time
- Divide
  16-bit by 8-bit, 16-bit quotient, 8-bit remainder
  Less than 14 μs execution-time
- Working register instructions for efficient RAM addressing, testing and manipulating
- Direct bit addressing for code-efficient addressing, testing and manipulating bits in RAM, port lines and mode registers

MEMORY MAP



In case of μPD7807
external ROM area is starting from 0000H
(no internal ROM area)

FUNCTIONAL DESCRIPTION

Please refer to the section of μPD7811 for description of the following functions which are the same as on this device:

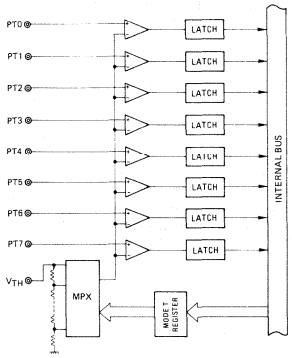
1. Memory expansion (except 56K bytes maximum for μPD7809)
2. USART
3. Reset
4. External memory access and timing

Variable Threshold Input Port (Port T)

- 8 input lines
- 16 levels – from 1/16 of reference voltage (V_{TH}) to 16/16 V_{TH}
- Level selected by software write to Mode T register
- Input at Port bit reads 0 until voltage at pin exceeds selected level
- Comparison execution time: 12 μs

FUNCTIONAL DESCRIPTION (CONT.)

Block Diagram of Treshold Variable Input Port



Format of MODE T Register

7	6	5	4	3	2	1	0
–	–	–	–	MT3	MT2	MT1	MT0

Specification of 16 Threshold Levels

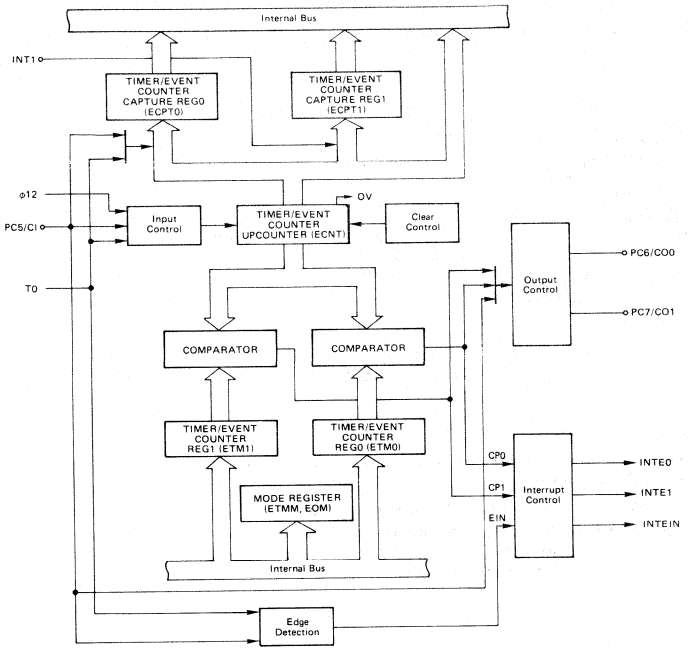
0	0	0	0	$V_{TH} \times 16/16$
0	0	0	1	$V_{TH} \times 1/16$
0	0	1	0	$V_{TH} \times 2/16$
0	0	1	1	$V_{TH} \times 3/16$
0	1	0	0	$V_{TH} \times 4/16$
0	1	0	1	$V_{TH} \times 5/16$
0	1	1	0	$V_{TH} \times 6/16$
0	1	1	1	$V_{TH} \times 7/16$
1	0	0	0	$V_{TH} \times 8/16$
1	0	0	1	$V_{TH} \times 9/16$
1	0	1	0	$V_{TH} \times 10/16$
1	0	1	1	$V_{TH} \times 11/16$
1	1	0	0	$V_{TH} \times 12/16$
1	1	0	1	$V_{TH} \times 13/16$
1	1	1	0	$V_{TH} \times 14/16$
1	1	1	1	$V_{TH} \times 15/16$

Input/Output

- 40 digital I/O lines – Five 8-bit ports (Port A, Port B, Port C, Port D, Port F)
- Port operation for Ports A, B, C and F: Each line of these ports can be individually programmed as an input or as an output
- Port D can be programmed as a byte input or a byte output
- Control lines: Under software control, each line of Port C can be configured individually to provide control lines for serial interface timer and timer/counter and interrupt.

FUNCTIONAL DESCRIPTION (CONT.)

TIMER / EVENT COUNTER – BLOCK DIAGRAM



Note: $\phi 12 = f_{XTAL} \times 1/12$,

f_{XTAL} : oscillation frequency

Input Clock of TIMER/EVENT COUNTER: Internal ($\phi 12$)
External (CI)
Timer out (TO)

Operations:

a) Interval Timer:
Counter repeats interruptions due to a present count time.

b) Event Count Mode:
CI inputs are synchr. by the internal clock. 250ns noise detection.

c) Frequency Measurement Mode:
CI inputs while TO is kept at high level.

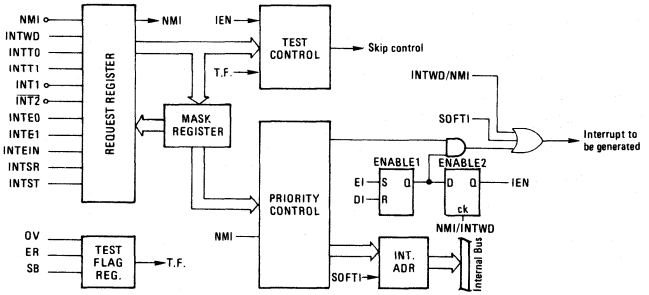
d) Puls with Meaurement Mode:
Counting up the upcounter during CI is high or low.

e) Programmable Square Wave:
Comperator 0 signal sets $CO_{0/1}$, Comperator 1 signal reset $CO_{0/1}$.

f) Single Pulse Generation:
CI is trigger input 16 bit counter free running output Flip-Flop toggled two times.

FUNCTIONAL DESCRIPTION (CONT.)

INTERRUPT CONTROL CIRCUITRY – BLOCK DIAGRAM



Mask register: Masking the interrupts

Priority control: Accepts only the interrupt with the highest priority if more than one request at the same time.

Test Flag register: 3 kinds of test flags which doesn't bring any interrupt request:

OV: set to 1 by overflow of the timer/event counter
ER: set to 1 by priority error
SB: set to 1 by rise input of V_{DD} terminal

INTERRUPT

11 Interrupt Sources

3 External Interrupts – Including non maskable interrupt
8 Internal Interrupts

6 Priority Levels and 6 Interrupt Vectors

11 Interrupt sources are divided into 6 priority levels.

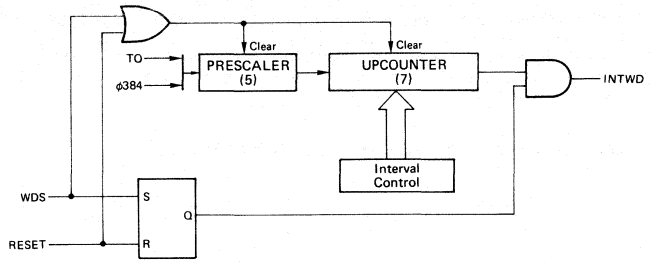
PRIORITY	INTERRUPT ADDRESS	INTERRUPT SOURCE		INTERNAL/ EXTERNAL
1	4 (0004H)	$\overline{\text{NMI}}$	falling edge	external
		INTWD	output signal of watchdog timer	internal
2	8 (0008H)	INTT0	coincidence signal from TIMER0	internal
		INTT1	coincidence signal from TIMER1	
3	16 (0010H)	INT1	rising edge	external
		$\overline{\text{INT2}}$	falling edge	
4	24 (0018H)	INTE0	coincidence signal from timer/ event counter	internal
		INTE1	coincidence signal from timer/ event counter	
5	32 (0020H)	INTEIN	falling edge of CI or TO	internal
6	40 (0028H)	INTSR	serial receive interrupt	internal
		INTST	serial transmit interrupt	

FUNCTIONAL DESCRIPTION (CONT.)

WATCHDOG TIMER

Used for software safety check or overall performance safety check. Watchdog, if enabled, must be cleared at regular intervals in program execution to avoid watchdog interrupt or by Reset. Intervals are software selectable.

BLOCK DIAGRAM OF WATCHDOG TIMER



Note: $\phi 384 = f_{XTAL} \times 1/384$

HOLD/HLDA

To perform all sorts of DMA-applications a Hold-request signal can be applied to the μPD7809; it puts Address- and Databus and RD/WR signal lines to the high impedance state. Then HLDA goes high as a response to the hold request.

MODE0/MODE1-TERMINALS

The logic level applied to M0/M1-Terminals determines the memory map of μPD7807/08/09 and the use of Port D/F as multiplexed Address/Data Bus.

M0	M1	MEMORY	ADDRESSES	LOCATION
0	1	8K/4K	0 . . . . . 0FFFH/1FFFH	internal*
0	0	4K	0 . . . . . .OFFFH	external
0	1	16K	0 . . . . . 3FFFH	external
1	0	64K	0 . . . . . FEFFH	external

* M0, M1 = 0,1 realizes the ROM version (access of internal ROM), all others represent access of external memory only. In case external memory is used in addition to internal, memory mapping register has to be programmed then (see below).

MEMORY EXPANDES MODES	MEMORY MAPPING REGISTER			NUMBER OF I/O LINES
	MM2	MM1	MM0	
Port Mode	0	0	X	44
256 Expanded	0	1	0	36
4K Expanded	1	0	0	32
16K Expanded	1	1	0	30
56K/60K* Expanded	1	1	1	28

*56K for 7809, 60K for 7808

FUNCTIONAL DESCRIPTIONS (CONT.)

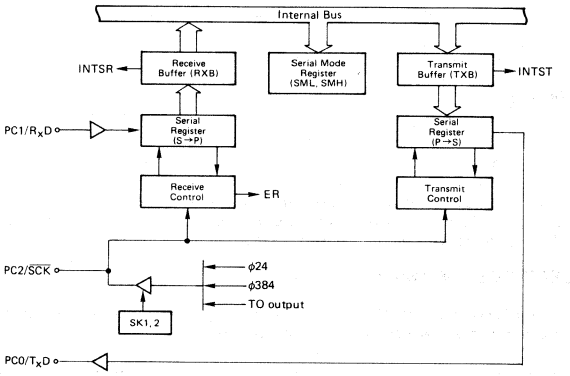
STANDBY FUNCTION

The μPD7809/08/07/P09 offers a standby function that allows the user to save up to 32 bytes of RAM with backup power (V_{DD}) if the main power (V_{CC}) fails. On powerup the μPD7809 checks whether recovery was made from standby mode or from cold start.

UNIVERSAL SERIAL INTERFACE

The serial interface can operate in any of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first for ease of communication with certain peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception. In the search mode, data is transferred one bit at a time from serial register to receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from serial register to transmit buffer occurs 8 bits at a time.

UNIVERSIAL SERIAL INTERFACE BLOCK DIAGRAM



Note: $\phi 24 = f_{XTAL} \times 1/24$

$\phi 384 = f_{XTAL} \times 1/384$ f_{XTAL}: oscillation frequency (MHz)

- Asynchronous Mode
  - Full-Duplex, Double Buffering
  - 7, 8-Bit/Character
  - Start/Stop Bit
  - Even/Odd Parity
  - Programmable Clock Rate X1, X16, X64
- Synchronous Mode
  - Search/Receive Mode
- I/O Interface Mode (μPD7801 Serial Mode)
- Programmable Communication Rate
  - 2μsec, 32μsec, Timer and External

FUNCTIONAL DESCRIPTION (CONT.)

ZERO-CROSSING DETECTOR

The INT1 and INT2 terminals (used common to TI and PC_3) can be used to detect the zero-crossing point of slow moving AC signals. When driven directly, these pins respond as a normal digital input.

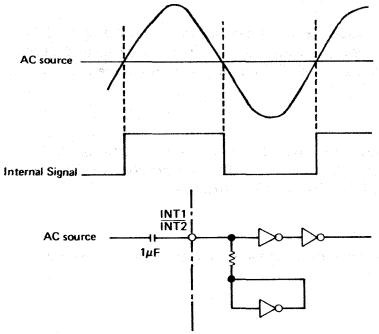
To utilize the zero-cross detection mode, an AC signal of approximately 1–3V AC peak-to-peak magnitude and a maximum frequency of 1kHz is coupled through an external capacitor to these pins.

For the INT1 pin, the internal digital state is sensed as a zero until the rising edge crosses the DC average level, when it becomes a one and INT1 interrupt is generated.

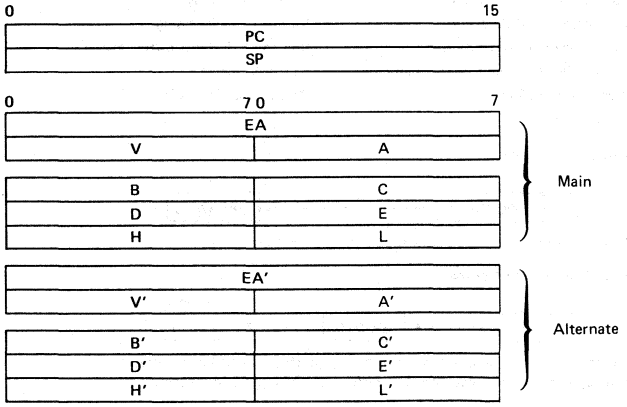
For the INT2 pin, the state is sensed as a one until the falling edge crosses the DC average level, when it becomes a zero and INT2 interrupt is generated.

The zero-cross detection capability allows the user to make the 50–60Hz power signal the basis for system timing and to control voltage phase sensitive devices.

ZERO-CROSSING DETECTION CIRCUIT



REGISTERS



FUNCTIONAL DESCRIPTION (CONT.)

General Purpose Registers (B, C, D, E, H. L)

There are two sets of general purpose registers (Main: B, C, D, E, H, L: Alternate: B', C', D', H', L'). They can function as auxiliary registers to the accumulator or in pairs as data pointers (BC, DE, HL, B'C', D'E', H'L'). Auto Increment and Decrement addressing mode capabilities extend the uses for the DE, HL, D'E', and H'L' register-pairs. The contents of the BC, DE, and HL register-pairs can be exchanged with their Alternate Register counterparts using the EXX instruction.

Vector Register (V)

When defining a scratch pad area in the memory space, the upper 8-bit memory address is defined in the V-register and the lower 8-bits is defined by the immediate data of an instruction. Also the scratch pad indicated by the V-register can be used as 256 x 8-bit working registers for storing software flags, parameters and counters.

Accumulator (A)

All data transfers between the μPD7809 and external memory of I/O are done through the accumulator. The contents of the Accumulator and Vector Registers can be exchanged with their Alternate Registers using the EX instruction.

Program Counter (PC)

The PC is a 16-bit register containing the address of the next instruction to be fetched. Under normal program flow, the PC is automatically incremented. However, in the case of a branch instruction, the PC contents are from another register or an instruction's immediate data. A reset sets the PC to 0000_H.

Stack Pointer (SP)

The stack pointer is a 16-bit register used to maintain the top of the stack area (last-in-first-out). The contents of the SP are decremented during a CALL or PUSH instruction or if an interrupt occurs. The SP is incremented during a RETURN or POP instruction.

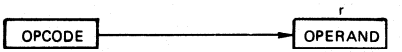
Extended Accumulator (EA)

The data processings of 16-bit arithmetic and logical operation instructions are mainly handled in the extended accumulator.

ADDRESS MODES

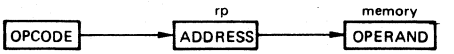
Register Addressing	Working Register Addressing
Register Indirect Addressing	Direct Addressing
Auto-Increment Addressing	Immediate Addressing
Auto-Decrement Addressing	Immediate Extended Addressing
Double Auto-Increment Addressing	Base Addressing
Relative Addressing	Base-Index-Addressing

Register Addressing



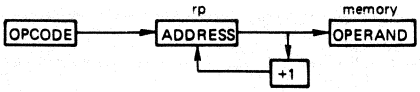
The instruction opcode specifies a register r which contains the operand.

Register Indirect Addressing



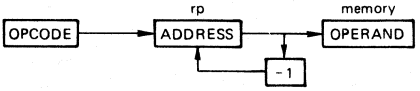
The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are ending this address mode.

Auto-Increment Addressing

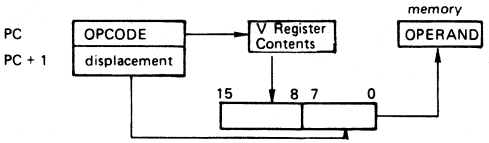


The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair is automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

Auto Decrement Addressing

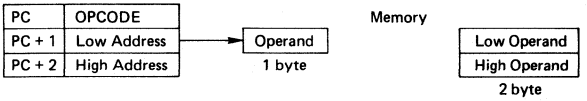


Working Register Addressing



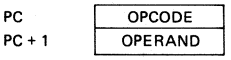
The contents of the register is linked with the byte following the opcode to form a memory address whose contents is the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only 1 additional byte is required for the address. Mnemonics with a W suffix ending this address mode.

Direct Addressing

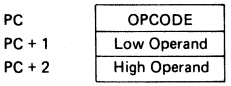


The two bytes following the opcode specify an address of a location containing the operand.

Immediate Addressing

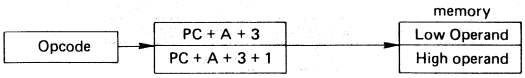


Immediate Extended Addressing



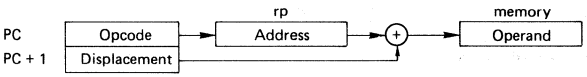
FUNCTIONAL DESCRIPTIONS (CONT.)

Relative Addressing



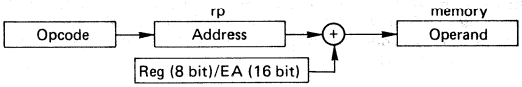
This addressing mode is used by the "Table"-command. It transfers the contents of 2 memory cells – addressed relatively to PC via the Accu A – into BC register-pair (TABLE-command). Application: Table look-up

Base-Addressing



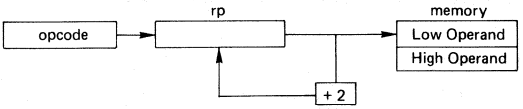
Register Pair DE or HL used as base pointer to the memory; immediate data (8 bit) or displacement added to the base.

Base-Index-Addressing



Register pair DE or HL used as base pointers to the memory; Register (8 bit) or Extended Accumulator (EA) as displacement added to the base.

Double auto increment



The opcode specifies the register pair which contains the memory address of the operand (16-bit). The contents of the register pair is automatically incremented by two to point to a new 16-bit operand.

FUNCTIONAL DESCRIPTION (CONT.)

BIT ADDRESS INSTRUCTIONS

The following bits may be addressed directly with certain instructions:

- Any bit in a 16-byte group in RAM
- Any bit in the five 8-bit I/O ports (A, B, C, D, F)
- Any bit in the variable threshold port
- Any bit in the following special registers:

  9-bit interrupt mask register, serial mode register, timer mode register, timer/event counter output register

An addressed bit may be tested, set, cleared, or complemented.
An addressed bit may be moved to or from the carry flag.
An addressed bit may be ANDed, ORed, X-ORed with the carry flag.

Difference between the μPD7801, μPD7811, μPD7807, and μPD7809

		μPD7801	μPD7811	μPD7807	μPD7809
Number of Instructions		134	158	165	165
16-Bit Operation Instruction		No	Yes	Yes	Yes
Multipy/Divide Instruction		No	Yes	Yes	Yes
Instruction Cycle		2μs/4MHz	1μs/12MHz	1μs/12MHz	1μs/12MHz
Number of General-purpose Registers		16	18	18	18
On-chip ROM Capacity		4K Bytes	4K Bytes	No	8K Bytes
On-chip RAM Capacity		128 Bytes	256 Bytes	256 Bytes	256 Bytes
Direct-Addressable External Memory Capacity		60K Bytes	60K Bytes	64K Bytes	56K Bytes
Interrupt Source	Internal	2	8	8	8
	External	3	3	3	3
I/O Lines		48	40+4	28*	40
Threshold Variable Port		No	No	8 Bits	8 Bits
Timer/Counter	Timer	12 Bits	8 Bits x 2	8 Bits x 2	8 Bits x 2
	Counter	No	16 Bits	16 Bits	16 Bits
Watchdog Timer		No	No	Yes	Yes
Serial Interface	Asynchronous	No	Yes	Yes	Yes
	Synchronous	No	Yes	Yes	Yes
	I/O Interface	Yes	Yes	Yes	Yes
A/D Converter		No	Yes	No	No
Standby Function		No	Yes	Yes	Yes
Hold Function		Yes	no	Yes	Yes
Technology		NMOS	NMOS	NMOS	NMOS
Package		64-Pin QUIP	64-Pin QUIP	64-Pin QUIP	64-Pin QUIP

*: at 4K-byte Access

OPERAND FORMAT/DESCRIPTION

FORMAT	DESCRIPTION
r r1 r2	V, A, B, C, D, E, H, L EAH, EAL, B, C, D, E, H, L A, B, C
sr sr1 sr2 sr3 sr4 sr5	PA, PB, PC, PD, PF, MKH, MKL, SMH, SML, EOM, ETMM, TMM, MM, MCC, MA, MB, MC, MF, TXB, TM0, TM1, WDM, MT PA, PB, PC, PD, PF, MKH, MKL, SMH, EOM, TMM, PT, RXB, WDM PA, PB, PC, PD, PF, MKH, MKL, SMH, EOM, TMM ETM0, ETM1 ECNT, ECPT0, ECPT1 PA, PB, PC, PD, PF, MKH, MKL, SMH, EOM, TMM, PT
rp rp1 rp2 rp3	SP, B, D, H V, B, D, H, EA SP, B, D, H, EA B, D, H
rpa rpa1 rpa2 rpa3	B, D, H, D+, H+, D–, H– B, D, H B, D, H, D+, H+, D–, H–, D+byte, H+A, H+B, H+EA, H+byte D, H, D++, H++, D+byte, H+A, H+B, H+EA, H+byte
wa	8 bit immediate data
word byte	16 bit immediate data 8 bit immediate data
bit	8 bit immediate data
f	CY, HC, Z
irf	FNMI, FT0, FT1, F1, F2, FE0, FE1, FEIN, FSR, FST, ER, OV, IFE2, SB

REMARKS

1. sr ~ sr5 (special register)

PA	:	PORT A
PB	:	PORT B
PC	:	PORT C
PD	:	PORT D
PF	:	PORT F
PT	:	PORT T
MA	:	MODE A
MB	:	MODE B
MC	:	MODE C
MCC	:	MODE CONTROL C
MF	:	MODE F
MM	:	MEMORY MAPPING
MT	:	MODE T
TM0	:	TIMER REG0
TM1	:	TIMER REG1
TMM	:	TIMER MODE
ETM0	:	TIMER/EVENT COUNTER REG0
ETM1	:	TIMER/EVENT COUNTER REG1
ECNT	:	TIMER/EVENT COUNTER UPCOUNTER
ECPT0	:	TIMER/EVENT COUNTER CAPTURE0
ECPT1	:	TIMER/EVENT COUNTER CAPTURE1
ETMM	:	TIMER/EVENT COUNTER MODE
EOM	:	TIMER/EVENT COUNTER OUTPUT MODE
WDM	:	WATCHDOG TIMER MODE
TXB	:	Tx BUFFER
RXB	:	Rx BUFFER
SMH	:	SERIAL MODE High
SML	:	SERIAL MODE Low
MKH	:	MASK High
MKL	:	MASK Low

2. rp ~ rp3 (register pair)

SP	:	STACK POINTER
B	:	BC
D	:	DE
H	:	HL
V	:	VA
EA	:	EXTENDED ACCUMULATOR

3. rpa ~ rpa3 (rp addressing)

B	:	(BC)
D	:	(DE)
H	:	(HL)
D+	:	(DE)+
H+	:	(HL)+
D−	:	(DE)−
H−	:	(HL)−
D++	:	(DE)++
H++	:	(HL)++
D+byte	:	(DE+byte)
H+A	:	(HL+A)
H+B	:	(HL+B)
H+EA	:	(HL+EA)
H+byte	:	(HL+byte)

4. f (flag)

CY	:	CARRY
HC	:	HALF CARRY
Z	:	ZERO

5. irf (interrupt flag)

FMMI	:	INTFNMI
FT0	:	INTFT0
FT1	:	INTFT1
F1	:	INTF1
F2	:	INTF2
FE0	:	INTFE0
FE1	:	INTFE1
FEIN	:	INTFEIN
FSR	:	INTFSR
FST	:	INTFST
ER	:	ERROR
OV	:	OVERFLOW
IEF2	:	INTERRUPT ENABLE F/F2
SB	:	STANDBY

Parts of this material may be changed without prior notice due to the introduction of new functions of products under development.

INSTRUCTION SET

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
8-BIT DATA TRANSFER	MOV		r1, A	00011 T_2 T_1 T_0				4	r1 ← A	
			A, r1	00001 T_2 T_1 T_0				4	A ← r1	
		*	sr, A	01001101	11 S_5 S_4 S_3 S_2 S_1 S_0			10	sr ← A	
		*	A, sr1	01001100	11 S_5 S_4 S_3 S_2 S_1 S_0			10	A ← sr1	
			r, word	01110000	01101 R_2 R_1 R_0	Low Adrs	High Adrs	17	r ← (word)	
			word, r	01110000	01111 R_2 R_1 R_0	Low Adrs	High Adrs	17	(word) ← r	
		*	r, byte	01101 R_2 R_1 R_0	Data			7	r ← byte	
	MVI		sr2, byte	01100100	S_3 0000 S_2 S_1 S_0	Data		14	sr2 ← byte	
	MVIW	*	wa, byte	01110001	Offset	Data		13	(V.wa) ← byte	
	MVIX	*	rpa1, byte	01001 A_1 A_0	Data			10	(rpa1) ← byte	
	STAW	*	wa	01100011	Offset			10	(V.wa) ← A	
	LDAW	*	wa	00000001	Offset			10	A ← (V.wa)	
	STAX	*	rpa2	A_3 0111 A_2 A_1 A_0	Data (*1)			7/13	(rpa2) ← A	
	LDAX	*	rpa2	A_3 0101 A_2 A_1 A_0	Data (*1)			7/13	A ← (rpa2)	
	EXX			01001000	10101111			8	B ↔ B', C ↔ C', D ↔ D', E ↔ E', H ↔ H', L ↔ L'	
	EXA			01001000	10101100			8	V, A ↔ V', A', EA ↔ EA'	
	EXH			01001000	10101110			8	H, L ↔ H', L'	
	EXR			01001000	10101101			8	V ↔ V', A ↔ A', B ↔ B', C ↔ C', D ↔ D', E ↔ E', H ↔ H', L ↔ L', EA ↔ EA'	

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
16-BIT DATA TRANSFER	BLOCK		D+	00010000				13* (C+1)	(DE)+ ← (HL)+, C ← C−1 End if borrow	
			D−	00010001				13* (C+1)	(DE)− ← (HL)−, C ← C−1 End if borrow	
	DMOV		rp3, EA	101101 P_1 P_0				4	$rp3_L$ ← EAL, $rp3_H$ ← EAH	
			EA, rp3	101001 P_1 P_0				4	EAL ← $rp3_L$, EAH ← $rp3_H$	
			sr3, EA	01001000	1101001 U_0			14	sr3 ← EA	
			EA, sr4	↓ ↓	110000 V_1 V_0			14	EA ← sr4	
	SBCD		word	01110000	00011110	Low Adrs	High Adrs	20	(word) ← C, (word+1) ← B	
	SDED		word	↓ ↓	00101110	↓	↓	20	(word) ← E, (word+1) ← D	
	SHLD		word	↓ ↓	00111110	↓	↓	20	(word) ← L, (word+1) ← H	
	SSPD		word	↓ ↓	00001110	↓	↓	20	(word) ← SP_L, (word+1) ← SP_H	
	STEAX		rpa3	01001000	1001 C_3 C_2 C_1 C_0	Data (*2)		14/20	(rpa3) ← EAL, (rpa3+1) ← EAH	
	LBCD		word	01110000	00011111	Low Adrs	High Adrs	20	C ← (word), B ← (word+1)	
	LDED		word	↓ ↓	00101111	↓	↓	20	E ← (word), D ← (word+1)	
	LHLD		word	↓ ↓	00111111	↓	↓	20	L ← (word), H ← (word+1)	
	LSPD		word	↓ ↓	00001111	↓	↓	20	SP_L ← (word), SP_H ← (word+1)	
	LDEAX		rpa3	01001000	1000 C_3 C_2 C_1 C_0	Data (*2)		14/20	EAL ← (rpa3), EAH ← (rpa3+1)	
	PUSH		rp1	10110 Q_2 Q_1 Q_0				13	(SP−1) ← $rp1_H$, (SP−2) ← $rp1_L$ SP ← SP−2	
	POP		rp1	10100 Q_2 Q_1 Q_0				10	$rp1_L$ ← (SP), $rp1_H$ ← (SP+1) SP ← SP+2	
	LXI	*	rp2, word	0 P_2 P_1 P_0 0100	Low Byte	High Byte		10	rp2 ← word	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
	TABLE		01001000	10101000			17	C ← (PC+3+A) B ← (PC+3+A+1)	
8-BIT ARITHMETIC (REGISTER)	ADD	A, r	01100000	11000 R_2 R_1 R_0			8	A ← A+r	
		r, A		01000 R_2 R_1 R_0			8	r ← r+A	
	ADC	A, r		11010 R_2 R_1 R_0			8	A ← A+r+CY	
		r, A		01010 R_2 R_1 R_0			8	r ← r+A+CY	
	ADDNC	A, r		10100 R_2 R_1 R_0			8	A ← A+r	No Carry
		r, A		00100 R_2 R_1 R_0			8	r ← r+A	No Carry
	SUB	A, r		11100 R_2 R_1 R_0			8	A ← A−r	
		r, A		01100 R_2 R_1 R_0			8	r ← r−A	
	SBB	A, r		11110 R_2 R_1 R_0			8	A ← A−r−CY	
		r, A		01110 R_2 R_1 R_0			8	r ← r−A−CY	
	SUBNB	A, r		10110 R_2 R_1 R_0			8	A ← A−r	No Borrow
		r, A		00110 R_2 R_1 R_0			8	r ← r−A	No Borrow
	ANA	A, r		10001 R_2 R_1 R_0			8	A ← A ∧ r	
		r, A		00001 R_2 R_1 R_0			8	r ← r ∧ A	
	ORA	A, r		10011 R_2 R_1 R_0			8	A ← A ∨ r	
		r, A		00011 R_2 R_1 R_0			8	r ← r ∨ A	
	XRA	A, r		10010 R_2 R_1 R_0			8	A ← A ⊻ r	
		r, A		00010 R_2 R_1 R_0			8	r ← r ⊻ A	
	GTA	A, r		10101 R_2 R_1 R_0			8	A−r−1	No Borrow
		r, A	▼ ▼	00101 R_2 R_1 R_0			8	r−A−1	No Borrow

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
8-BIT ARITHMETIC (REG.)	LTA	A, r	01100000	10111 R_2 R_1 R_0			8	A−r	Borrow
		r, A		00111 R_2 R_1 R_0			8	r−A	Borrow
	NEA	A, r		11101 R_2 R_1 R_0			8	A−r	No Zero
		r, A		01101 R_2 R_1 R_0			8	r−A	No Zero
	EQA	A, r		11111 R_2 R_1 R_0			8	A−r	Zero
		r, A		01111 R_2 R_1 R_0			8	r−A	Zero
	ONA	A, r		11001 R_2 R_1 R_0			8	A ∧ r	No Zero
	OFFA	A, r	▼ ▼	11011 R_2 R_1 R_0			8	A ∧ r	Zero
8-BIT ARITHMETIC (MEMORY)	ADDX	rpa	01110000	11000 A_2 A_1 A_0			11	A ← A+ (rpa)	
	ADCX	rpa		11010 A_2 A_1 A_0			11	A ← A+ (rpa)+CY	
	ADDNCX	rpa		10100 A_2 A_1 A_0			11	A ← A+ (rpa)	No Carry
	SUBX	rpa		11100 A_2 A_1 A_0			11	A ← A− (rpa)	
	SBBX	rpa		11110 A_2 A_1 A_0			11	A ← A− (rpa)−CY	
	SUBNBX	rpa		10110 A_2 A_1 A_0			11	A ← A− (rpa)	No Borrow
	ANAX	rpa		10001 A_2 A_1 A_0			11	A ← A ∧ (rpa)	
	ORAX	rpa		10011 A_2 A_1 A_0			11	A ← A ∨ (rpa)	
	XRAX	rpa		10010 A_2 A_1 A_0			11	A ← A ⊻ (rpa)	
	GTAX	rpa		10101 A_2 A_1 A_0			11	A− (rpa)−1	No Borrow
	LTAX	rpa	▼ ▼	10111 A_2 A_1 A_0			11	A− (rpa)	Borrow

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	NEAX		rpa	01110000	11101 A_2 A_1 A_0			11	A ← (rpa)	No Zero
	EQAX		rpa		11111 A_2 A_1 A_0			11	A ← (rpa)	Zero
	ONAX		rpa		11001 A_2 A_1 A_0			11	A ∧ (rpa)	No Zero
	OFFAX		rpa	↓	11011 A_2 A_1 A_0			11	A ∧ (rpa)	Zero
	ADI	•	A, byte	01000110	← Data →			7	A ← A+byte	
			r, byte	01110100	01000 R_2 R_1 R_0	Data		11	r ← r+byte	
			sr2, byte	01100100	S_3 1000 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte	
	ACI	•	A, byte	01010110	← Data →			7	A ← A+byte+CY	
			r, byte	01110100	01010 R_2 R_1 R_0	Data		11	r ← r+byte+CY	
			sr2, byte	01100100	S_3 1010 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte+CY	
	ADINC	•	A, byte	00100110	← Data →			7	A ← A+byte	No Carry
			r, byte	01110100	00100 R_2 R_1 R_0	Data		11	r ← r+byte	No Carry
			sr2, byte	01100100	S_3 0100 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte	No Carry
	SUI	•	A, byte	01100110	← Data →			7	A ← A−byte	
			r, byte	01110100	01100 R_2 R_1 R_0	Data		11	r ← r−byte	
			sr2, byte	01100100	S_3 1100 S_2 S_1 S_0	↓		20	sr2 ← sr2−byte	
	SBI	•	A, byte	01110110	← Data →			7	A ← A−byte−CY	
			r, byte	01110100	01110 R_2 R_1 R_0	Data		11	r ← r−byte−CY	
			sr2, byte	01100100	S_3 1110 S_2 S_1 S_0	↓		20	sr2 ← sr2−byte−CY	

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	SUINB	•	A, byte	00110110	← Data →			7	A ← A−byte	No Borrow
			r, byte	01110100	00110 R_2 R_1 R_0	Data		11	r ← r−byte	No Borrow
			sr2, byte	0110 ↓	S_3 0110 S_2 S_1 S_0	↓		20	sr2 ← sr2−byte	No Borrow
	ANI	•	A, byte	00000111	← Data →			7	A ← A ∧ byte	
			r, byte	01110100	00001 R_2 R_1 R_0	Data		11	r ← r ∧ byte	
			sr2, byte	01100100	S_3 0001 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∧ byte	
	ORI	•	A, byte	00010111	← Data →			7	A ← A ∨ byte	
			r, byte	01110100	00011 R_2 R_1 R_0	Data		11	r ← r ∨ byte	
			sr2, byte	0110 ↓	S_3 0011 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∨ byte	
	XRI	•	A, byte	00010110	← Data →			7	A ← A ∨ byte	
			r, byte	01110100	00010 R_2 R_1 R_0	Data		11	r ← r ∨ byte	
			sr2, byte	0110 ↓	S_3 0010 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∨ byte	
	GTI	•	A, byte	00100111	← Data →			7	A−byte−1	No Borrow
			r, byte	01110100	00101 R_2 R_1 R_0	Data		11	r−byte−1	No Borrow
			sr5, byte	0110 ↓	S_3 0101 S_2 S_1 S_0	↓		14	sr5−byte−1	No Borrow
	LTI	•	A, byte	00110111	← Data →			7	A−byte	Borrow
			r, byte	01110100	00111 R_2 R_1 R_0	Data		11	r−byte	Borrow
			sr5, byte	0110 ↓	S_3 0111 S_2 S_1 S_0	↓		14	sr5−byte	Borrow

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	* NEI	A, byte	01100111	← Data →			7	A–byte	No Zero
		r, byte	01110100	01101 R_2 R_1 R_0	Data		11	r–byte	No Zero
		sr5, byte	0110 ↓	S_3 1101 S_2 S_1 S_0	↓		14	sr5–byte	No Zero
	* EQI	A, byte	01110111	← Data →			7	A–byte	Zero
		r, byte	01110100	01111 R_2 R_1 R_0	Data		11	r–byte	Zero
		sr5, byte	0110 ↓	S_3 1111 S_2 S_1 S_0	↓		14	sr5–byte	Zero
	* ONI	A, byte	01000111	← Data →			7	A ∧ byte	No Zero
		r, byte	01110100	01001 R_2 R_1 R_0	Data		11	r ∧ byte	No Zero
		sr5, byte	0110 ↓	S_3 1001 S_2 S_1 S_0	↓		14	sr5 ∧ byte	No Zero
	* OFFI	A, byte	01010111	← Data →			7	A ∧ byte	Zero
		r, byte	01110100	01011 R_2 R_1 R_0	Data		11	r ∧ byte	Zero
		sr5, byte	0110 ↓	S_3 1011 S_2 S_1 S_0	↓		14	sr5 ∧ byte	Zero
WORKING REGISTER	ADDW	wa	01110100	11000000	Offset		14	A ← A+(V.wa)	
	ADCW	wa		1101			14	A ← A+(V.wa)+CY	
	ADDNCW	wa		1010			14	A ← A+(V.wa)	No Carry
	SUBW	wa		1110			14	A ← A–(V.wa)	
	SBBW	wa		1111			14	A ← A–(V.wa)–CY	
	SUBNBW	wa		1011 ↓			14	A ← A–(V.wa)	No Borrow
	ANAW	wa		10001000			14	A ← A ∧ (V.wa)	
	ORAW	wa	↓ ↓	1001 ↓	↓		14	A ← A ∨ (V.wa)	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
WORKING REGISTER	XRAM	wa	01110100	10010000	Offset		14	A ← A ∨ (V.wa)	
	GTAW	wa		10101000			14	A–(V.wa)–1	No Borrow
	LTAW	wa		1011			14	A–(V.wa)	Borrow
	NEAW	wa		1110			14	A–(V.wa)	No Zero
	EQAW	wa		1111			14	A–(V.wa)	Zero
	ONAW	wa		1100			14	A ∧ (V.wa)	No Zero
	OFFAW	wa	↓ ↓	1101 ↓	↓		14	A ∧ (V.wa)	Zero
	* ANIW	wa, byte	00000101	← Offset →	Data		19	(V.wa) ← (V.wa) ∧ byte	
	* ORIW	wa, byte	0001				19	(V.wa) ← (V.wa) ∨ byte	
	* GTIW	wa, byte	0010				13	(V.wa)–byte–1	No Borrow
	* LTIW	wa, byte	0011				13	(V.wa)–byte	Borrow
	* NEIW	wa, byte	0110				13	(V.wa)–byte	No Zero
	* EQIW	wa, byte	0111				13	(V.wa)–byte	Zero
	* ONIW	wa, byte	0100				13	(V.wa) ∧ byte	No Zero
	* OFFIW	wa, byte	0101 ↓	↓	↓		13	(V.wa) ∧ byte	Zero
16-BIT ARITHMETIC	EADD	EA, r2	01110000	01000 0 R_1 R_0			11	EA ← EA+r2	
	DADD	EA, rp3	0100	11001 P_1 P_0			11	EA ← EA+rp3	
	DADC	EA, rp3		1101			11	EA ← EA+rp3+CY	
	DADDNC	EA, rp3		1010 ↓			11	EA ← EA+rp3	No Carry
	ESUB	EA, r2	↓ 0000	011000 R_1 R_0			11	EA ← EA–r2	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
16-BIT ARITHMETIC	DSUB	EA, rp3	01110100	11100P_1 P_0			11	EA ← EA−rp3	
	DSBB	EA, rp3		1111			11	EA ← EA−rp3−CY	
	DSUBNB	EA, rp3		1011			11	EA ← EA−rp3	No Borrow
	DAN	EA, rp3		100011P_1 P_0			11	EA ← EA ∧ rp3	
	DOR	EA, rp3		1001			11	EA ← EA ∨ rp3	
	DXR	EA, rp3		100101P_1 P_0			11	EA ← EA ⊻ rp3	
	DGT	EA, rp3		101011P_1 P_0			11	EA−rp3−1	No Borrow
	DLT	EA, rp3		1011			11	EA−rp3	Borrow
	DNE	EA, rp3		1110			11	EA−rp3	No Zero
	DEQ	EA, rp3		1111			11	EA−rp3	Zero
	DON	EA, rp3		1100			11	EA ∧ rp3	No Zero
	DOFF	EA, rp3		1101			11	EA ∧ rp3	Zero
MULTIP/ DIVIDE	MUL	r2	01001000	001011R_1 R_0			32	EA ← A X r2	
	DIV	r2		0011			59	EA ← EA÷r2, r2 ← surplus	
INCREMENT/ DECREMENT	INR	r2	01000R_1 R_0				4	r2−r2+1	Carry
	INRW *	wa	00100000	← Offset →			16	(V.wa) ← (V.wa)+1	Carry
	INX	rp	00P_1 $P_0$0010				7	rp ← rp+1	
		EA	10101000				7	EA ← EA+1	
	DCR	r2	01010R_1 R_0				4	r2 ← r2−1	Borrow
	DCRW *	wa	00110000	← Offset →			16	(V.wa) ← (V.wa)−1	Borrow

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
	DCX	rp	00P_1 $P_0$0011				7	rp ← rp−1	
		EA	10101001				7	EA ← EA−1	
BIT MANIPULATION	MOV *	CY, bit	01011111	Bit Adrs			10	CY ← (bit)	
		bit,CY	01011010				13	(bit) ← CY	
	AND *	CY, bit	00110001				10	CY ← CY ∧ (bit)	
	OR *	CY, bit	01011100				10	CY ← CY ∨ (bit)	
	XOR *	CY, bit	01011110				10	CY ← CY ⊻ (bit)	
	SETB *	bit	01011000				13	(bit) ← 1	
	CLR *	bit	01011011				13	(bit) ← 0	
	NOT *	bit	01011001				13	(bit) ← $\overline{(bit)}$	
	SK *	bit	01011101				10	Skip if (bit)=1	(bit)=1
	SKN *	bit	01010000				10	Skip if (bit)=0	(bit)=0
OTHERS	DAA		01100001				4	Decimal Adjust Accumulator	
	STC		01001000	00101011			8	CY ← 1	
	CLC			00101010			8	CY ← 0	
	CMC		01001000	10101010			8	CY ← $\overline{CY}$	
	NEGA			00111010			8	A ← A+1	
ROTAT/ SHIFT	RLD		01001000	00111000			17	Rotate Left Digit	
	RRD			1001			17	Rotate Right Digit	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
ROTATE AND SHIFT	RLL	r2	01001000	00110 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow CY$, $CY \leftarrow r2_7$	
	RLR	r2		00 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow CY$, $CY \leftarrow r2_0$	
	SLL	r2		00100 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow 0$, $CY \leftarrow r2_7$	
	SLR	r2		00 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow 0$, $CY \leftarrow r2_0$	
	SLLC	r2		00000 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow 0$, $CY \leftarrow r2_7$	Carry
	SLRC	r2		00 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow 0$, $CY \leftarrow r2_0$	Carry
	DRLL	EA	10110100				8	$EA_{n+1} \leftarrow EA_n$, $EA_0 \leftarrow CY$, $CY \leftarrow EA_{15}$	
	DRLR	EA		0000			8	$EA_{n-1} \leftarrow EA_n$, $EA_{15} \leftarrow CY$, $CY \leftarrow EA_0$	
	DSLL	EA	10100100				8	$EA_{n+1} \leftarrow EA_n$, $EA_0 \leftarrow 0$, $CY \leftarrow EA_{15}$	
	DSLR	EA		0000			8	$EA_{n-1} \leftarrow EA_n$, $EA_{15} \leftarrow 0$, $CY \leftarrow EA_0$	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
JUMP	JMP *	word	01010100	← Low Adrs →	High Adrs		10	PC ← word	
	JB		00100001				4	$PC_H \leftarrow B$, $PC_L \leftarrow C$	
	JR	word	11 ← jdispl →				10	PC ← PC+1+jdispl	
	JRE *	word	0100111 ← jdisp →				10	PC ← PC+2+jdispl	
	JEA		01001000	00101000			8	PC ← EA	
CALL	CALL *	word	01000000	← Low adrs →	High Adrs		16	$(SP-1) \leftarrow (PC+3)_H$, $(SP-2) \leftarrow (PC+3)_L$, PC ← word, SP ← SP−2	
	CALB		01001000	00101001			17	$(SP-1) \leftarrow (PC+2)_H$, $(SP-2) \leftarrow (PC+2)_L$, $PC_H \leftarrow B$, SP ← SP−2	
	CALF *	word	01111 ← fa →				13	$(SP-1) \leftarrow (PC+2)_H$, $(SP-2) \leftarrow (PC+2)_L$, $PC_{15-11} \leftarrow 00001$, $PC_{10-0} \leftarrow$ fa, SP ← SP−2	
	CALT	word	100 ← ta →				16	$(SP-1) \leftarrow (PC+1)_H$, $(SP-2) \leftarrow (PC+1)_L$, $PC_L \leftarrow (128+2ta)$, $PC_H \leftarrow (129+2ta)$, SP ← SP−2	
	SOFTI		01110010				16	$(SP-1) \leftarrow PSW$, $(SP-2) \leftarrow (PC+1)_H$, $(SP-3) \leftarrow (PC+1)_L$, PC ← 0060H, SP ← SP−3	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
RETURN	RET		10111000				10	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$ SP ← SP+2	
	RETS		1001				10	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$ SP ← SP+2, PC ← PC+n	
	RETI		01100010				13	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$ PSW ← (SP+2), SP ← SP+3	Unconditional Skip
SKIP	SK	f	01001000	00001 F_2 F_1 F_0			8	Skip if f=1	f=1
	SKN	f		0001			8	Skip if f=0	f=0
	SKIT	irf		010 I_4 I_3 I_2 I_1 I_0			8	Skip if irf=1, then reset irf	irf=1
	SKNIT	irf		011 I_4 I_3 I_2 I_1 I_0			8	Skip if irf=0 Reset irf, if irf=1	irf=0
CPU CONTROL	NOP		00000000				4	No Operation	
	EI		10101010				4	Enable Interrupt	
	DI		10111010				4	Disable Interrupt	
	HLT		01001000	00111011			11	Halt	

Notes:

(*1): B2(Data) : rpa2 = D+byte, H+byte
(*2): B3(Data) : rpa3 = D+byte, H+byte
(*3): right side of slash (/) in states indicates case rpa2, rpa3 = D+byte, H+A, H+B, H+EA, H+byte
(*4): in the case of skip condition, the idle states are as follows.

1-byte instruction : 4 states — 2-byte instruction (with *) : 7 states
2-byte instruction : 8 states — 3-byte instruction (with *) : 10 states
3-byte instruction : 11 states — 4-byte instruction : 14 states

ELECTRICAL SPECIFICATIONS AND PACKAGE OUTLINES FOR μPD7807/μPD7808

ABSOLUTE MAXIMUM RATINGS

(T_a = 25° C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNITS
Power Supply Voltage	V_{CC}		−0.5 to +7.0	V
	V_{DD}		−0.5 to +7.0	V
Input Voltage	V_I		−0.5 to +7.0	V
Output Voltage	V_O		−0.5 to + 7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−0.5	mA
		All Output Pin Total	−20	mA
Threshold Voltage	V_{TH}		−0.5 to V_{CC} + 0.1	V
Operating Temperature	T_{opt}	10 MHz < f_{XTAL} ≤ 12 MHz	−10 to +70	°C
		f_{XTAL} ≤ 10 MHz	−40 to +85	°C
Storage Temperature	T_{stg}		−65 to + 150	°C

OPERATING CONDITION

OSC. FREQ. \ PARAMETER	T_a	V_{CC}, AV_{CC}
10 MHz < f_{XTAL} ≤ 12 MHz *1	−10°C to +70°C	+5.0V ± 5 %
f_{XTAL} ≤ 10 MHz *1	−40°C to +85°C	+5.0V ± 10 %

CAPACITANCE

(T_a = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_c = 1 MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	$C_{I/O}$				20	pF

DC CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1 *8	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ V_I ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) 0V ≤ V_I ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	+0.45V ≤ V_O ≤ V_{CC}			± 10	μA
V_{TH} Input Current	I_{TH}	V_{TH} = V_{CC}		0.2*2	0.5	mA
V_{DD} Supply Current	I_{DD}			1.5 *2	3.2	mA
V_{CC} Supply Current	I_{CC}			150*2	200	mA

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		83	250	ns
Address Setup to ALE ↓	t_{AL}	*3, *5	65		ns
Address Hold from ALE ↓	t_{LA}	*3, *5	50		ns
Address to $\overline{RD}$ ↓ Delay Time	t_{AR}	*3, *5	150		ns
$\overline{RD}$ ↓ to Address Floating	t_{AFR}	*5		20	ns
Address to Data Input	t_{AD}	*3, *5		360	ns
ALE ↓ to Data Input	t_{LDR}	*3, *5		215	ns
$\overline{RD}$ ↓ to Data Input	t_{RD}	*3, *5		180	ns
ALE ↓ to $\overline{RD}$ ↓ Delay Time	t_{LR}	*3, *5	35		ns
Data Hold Time from $\overline{RD}$ ↑	t_{RDH}	*5	0		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{RL}	*3, *5	115		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read *3, *5	280		ns
		OP Code Fetch *3, *5	530		ns
ALE Width High	t_{LL}	*3, *5	125		ns
$\overline{M1}$ Setup Time to $\overline{ALE}$ ↓	t_{ML}	*3	65		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*3	50		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*3	65		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*3	50		ns
Address to $\overline{WR}$ ↓ Delay	t_{AW}	*3, *5	150		ns
ALE ↓ to Data Output	t_{LDW}	*3, *5		195	ns
$\overline{WR}$ ↓ to Data Output	t_{WD}	*5		100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time	t_{LW}	*3, *5	35		ns
Data Setup Time to $\overline{WR}$ ↑	t_{DW}	*3, *5	230		ns
Data Hold Time from $\overline{WR}$ ↑	t_{WDH}	*3, *5	95		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{WL}	*3, *5	115		ns
$\overline{WR}$ Width Low	t_{WW}	*3, *5	280		ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*6	1		μs
			*7	500		ns
		$\overline{SCK}$ Output		2		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*6	420		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*6	420		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*6		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*6		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*6			210	ns

DC CHARACTERISTICS

(T_a = −40°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1 *8	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ V_I ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3); 0V ≤ V_I ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	+0.45V ≤ V_O ≤ V_{CC}			± 10	μA
V_{TH} Input Current	I_{TH}	V_{TH} = V_{CC}		0.2*2	0.6	mA
V_{DD} Supply Current	I_{DD}			1.5 *2	3.5	mA
V_{CC} Supply Current	I_{CC}			150*2	220	mA

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = −40°C to + 85°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		100	250	ns
Address Setup to ALE ↓	t_{AL}	*4, *5	100		ns
Address Hold from ALE ↓	t_{LA}	*4, *5	70		ns
Address to $\overline{RD}$ ↓ Delay Time	t_{AR}	*4, *5	200		ns
$\overline{RD}$ ↓ to Address Floating	t_{AFR}	*5		20	ns
Address to Data Input	t_{AD}	*4, *5		480	ns
ALE ↓ to Data Input	t_{LDR}	*4, *5		300	ns
$\overline{RD}$ ↓ to Data Input	t_{RD}	*4, *5		250	ns
ALE ↓ to $\overline{RD}$ ↓ Delay Time	t_{LR}	*4, *5	50		ns
Data Hold Time from $\overline{RD}$ ↑	t_{RDH}	*5	0		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{RL}	*4, *5	150		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read *4, *5	350		ns
		OP Code Fetch *4, *5	650		ns
ALE Width High	t_{LL}	*4, *5	160		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}	*4	100		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*4	70		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*4	100		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*4	70		ns
Address to $\overline{WR}$ ↓ Delay	t_{AW}	*4, *5	200		ns
ALE ↓ to Data Output	t_{LDW}	*4, *5		210	ns
$\overline{WR}$ ↓ to Data Output	t_{WD}	*5		100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time	t_{LW}	*4, *5	50		ns
Data Setup Time to $\overline{WR}$ ↑	t_{DW}	*4, *5	300		ns
Data Hold Time from $\overline{WR}$ ↑	t_{WDH}	*4, *5	130		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{WL}	*4, *5	150		ns
$\overline{WR}$ Width Low	t_{WW}	*4, *5	350		ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*6	1.2		μs
			*7	500		ns
		$\overline{SCK}$ Output		2.4		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*6	505		ns
			*7	200		ns
		$\overline{SCK}$ Output		1.1		μs
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*6	505		ns
			*7	200		ns
		$\overline{SCK}$ Output		1.1		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*6		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*6		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*6			210	ns

HOLD OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

(T_a = −40°C to + 85°C V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
HOLD ↑ Setup Time to ALE ↑	t_{SHDL}		2T + 150			ns
ALE ↑ to HLDA ↑ Delay	t_{DLHA}				T + 150	ns
HLDA ↑ to BUS Floating	t_{FBHA}		0			ns
HOLD ↓ to HLDA ↓ Delay	t_{HDDA}		T −50		4T + 150	ns
HLDA ↓ to Bus Enable Time	t_{EHAB}		0			ns
Bus Setup Time to ALE	t_{BL}		2T −100			ns

COMPARATOR CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Comparison Accuracy	V_{ACOMP}				± 100	mV
Threshold Voltage	V_{TH}		0		V_{CC}+0.1	V
Comparison Time	t_{COMP}		144		145	T_{CYC}
PT Input Voltage	V_{IPT}		0		V_{CC}	V

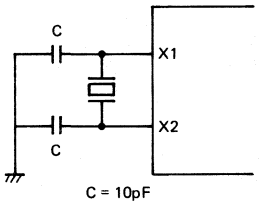
ZERO-CROSS CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

(T_a = −40°C to + 85°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

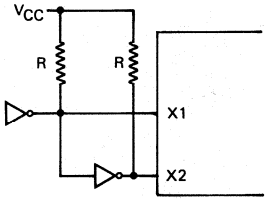
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

*1: XTAL oscillation circuit



C = 10pF

*8: External clock drive circuit



R = 5KΩ

*2: T_a = +25°C, V_{CC} = V_{DD} = 5V

*3: f_{XTAL} = 12 MHz

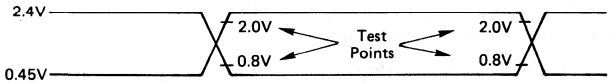
*4: f_{XTAL} = 10 MHz

*5: Load Capacitance: C_L = 150 pF

*6: Asynchronous mode with 1x baud rate, synchronous, I/O interface mode

*7: Asynchronous mode with 16x or 64x baud rate

AC TIMING TEST POINTS



EXTERNAL CLOCK

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

(T_a = −40°C to + 85°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
High Level Width	$t_{\phi H}$		30	250	ns
Low Level Width	$t_{\phi L}$		30	250	ns
Rising Time	t_r		0	30	ns
Falling Time	t_f		0	30	ns

DATA RETENTION CHARACTERISTICS

(T_a = −10 to +70°C, V_{CC} = 0V, V_{DD} = V_{DDDR})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Voltage	V_{DDDR}	RESET = V_{IL}	3.2		5.5	V
Data Retention Supply Current	I_{DDDR}	RESET = V_{IL}, V_{DDDR} = 3.2 V		1.3	3.0	mA

BUS TIMING DEPENDING ON tCYC

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNITS
t_{AL}	2T − 100	MIN	ns
t_{LA}	T − 30	MIN	ns
t_{AR}	3T − 100	MIN	ns
t_{AD}	7T − 220 *1	MAX	ns
t_{LDR}	5T − 200 *1	MAX	ns
t_{RD}	4T − 150 *1	MAX	ns
t_{LR}	T − 50	MIN	ns
t_{RL}	2T − 50	MIN	ns
t_{RR}	4T − 50 (Data Read) *1	MIN	ns
	7T − 50 (OP Code Fetch) *1		
t_{LL}	2T − 40	MIN	ns
t_{ML}	2T − 100	MIN	ns
t_{LM}	T − 30	MIN	ns
t_{IL}	2T − 100	MIN	ns
t_{LI}	T − 30	MIN	ns
t_{AW}	3T − 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T − 50	MIN	ns
t_{DW}	4T − 100 *1	MIN	ns
t_{WDH}	2T − 70	MIN	ns
t_{WL}	2T − 50	MIN	ns
t_{WW}	4T − 50 *1	MIN	ns
t_{CYK}	12T ($\overline{SCK}$ Input) *2	MIN	ns
	24T ($\overline{SCK}$ Output)		
t_{KKL}	5T + 5 (SCK Input) *2	MIN	ns
	12T − 100 ($\overline{SCK}$ Output)		
t_{KKH}	5T + 5 (SCK Input) *2	MIN	ns
	12T − 100 ($\overline{SCK}$ Output)		

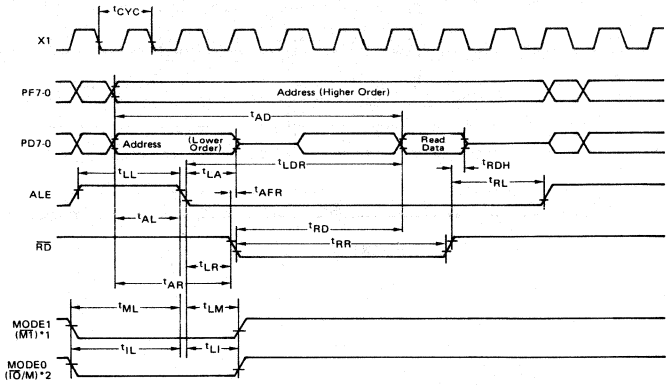
*1: Add 3T to each parameter in the case of external memory access using program WAIT function.

*2: Asynchronous mode with 1x baud rate, Synchronous, I/O Interface Mode

*3: T = t_{CYC} = 1/f_{XTAL}

*4: The items out of this table are not dependent on f_{XTAL}.

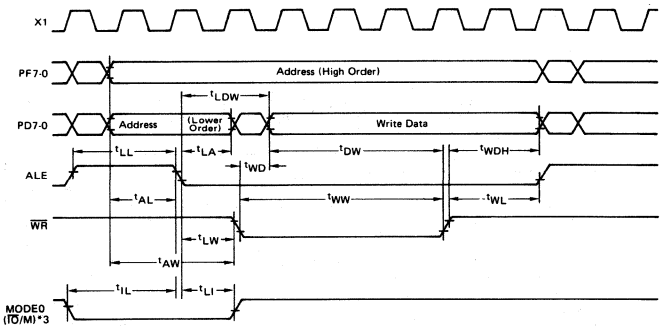
READ OPERATION



*1: $\overline{M1}$ signal is output to the MODE1 pin at 1st OP code fetch cycle when MODE 1 pin is pulled-up to V_{CC}.

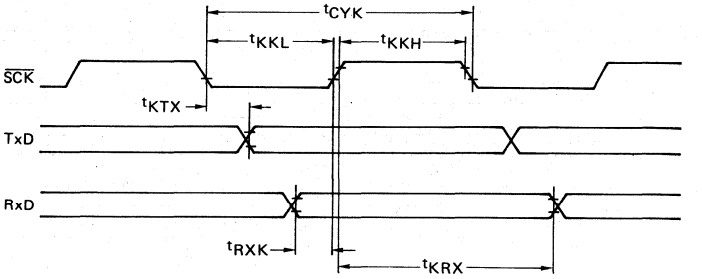
*2: $\overline{IO}$/M signal is output to the MODE0 pin at sr to sr2 register read timing when MODE0 pin is pulled-up to V_{CC}.

WRITE OPERATION

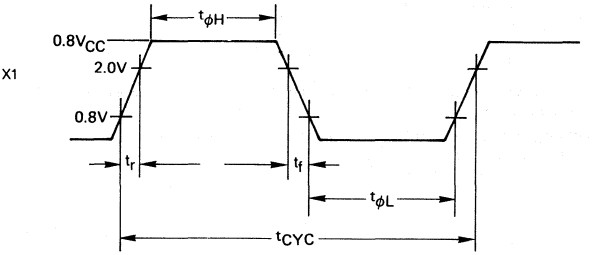


*3: $\overline{IO}$/M signal is output to the MODE0 pin at sr to sr2 register write timing when MODE0 pin is pulled-up to V_{CC}.

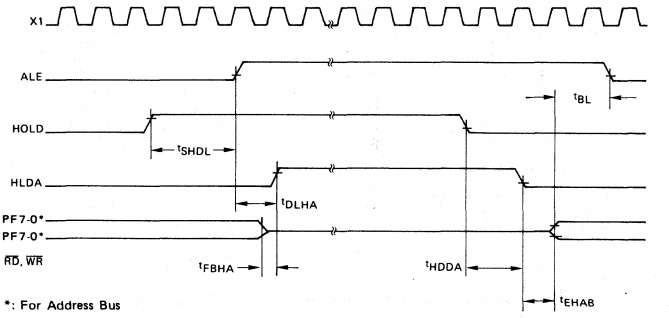
SERIAL OPERATION



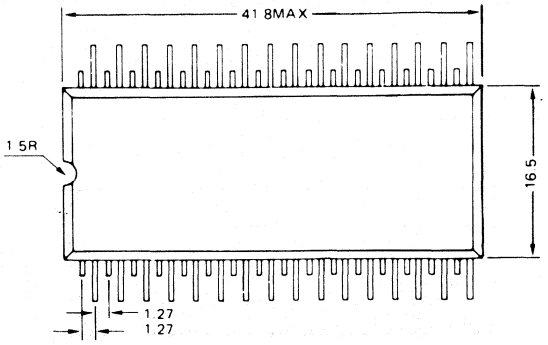
X1 INPUT WAVEFORM

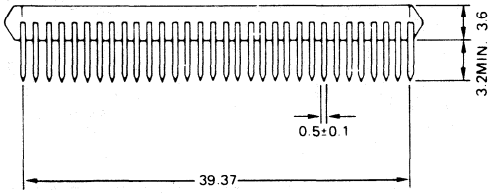


HOLD OPERATION

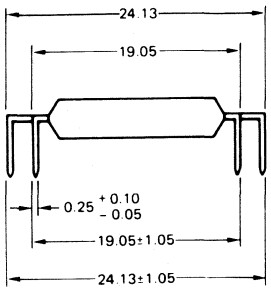


64 PIN PLASTIC
QUIP OUTLINE BENT LEADS
(Unit : mm)
μPD7807G/μPD7808G

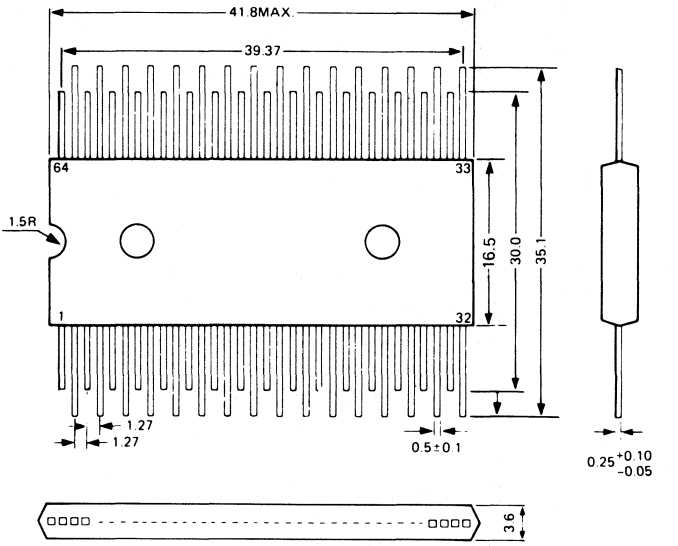




When ordering this package, specify as follows:
μPD7807G-36
μPD7808G-xxx-36



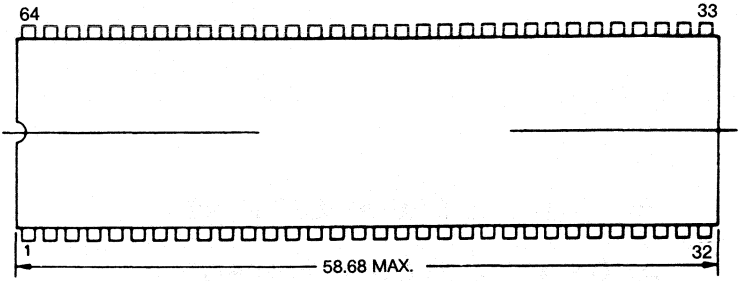
64 PIN PLASTIC QUIP
PACKAGE OUTLINE
STRAIGHT LEADS
(Unit : mm)
μPD7808



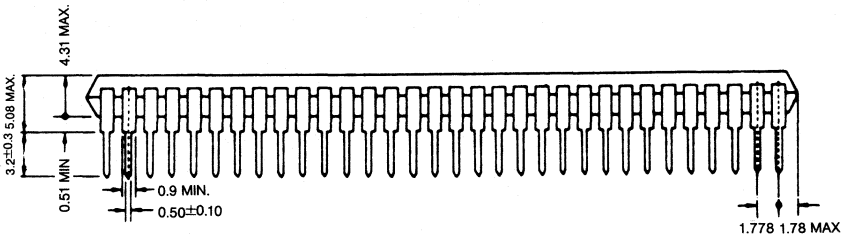
When ordering this package, specify as follows μPD7808G-xxx-37

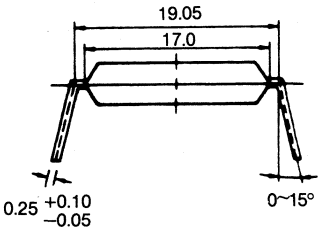
PACKAGE OUTLINE
μPD7807CW
μPD7808CW

64-PIN SHRINK DIP



When ordering this package, specify as follows:
μPD7807CW
μPD7808CW-xxx





ELECTRICAL SPECIFICATIONS

AND PACKAGE OUTLINES FOR

μPD7809

ABSOLUTE MAXIMUM RATINGS

(T_a = 25° C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNITS
Power Supply Voltage	V_{CC}		−0.5 to +7.0	V
	V_{DD}		−0.5 to +7.0	V
Input Voltage	V_I		−0.5 to +7.0	V
Output Voltage	V_O		−0.5 to + 7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−0.5	mA
		All Output Pin Total	−20	mA
Threshold Voltage	V_{TH}		−0.5 to V_{CC} + 0.1	V
Operating Temperature	T_{opt}	10 MHz < f_{XTAL} ≤ 12 MHz	−10 to +70	°C
		f_{XTAL} ≤ 10 MHz	−10 to +70	°C
Storage Temperature	T_{stg}		−40 to + 125	°C

OPERATING CONDITION

OSC. FREQ. \ PARAMETER	T_a	V_{CC}, AV_{CC}
10 MHz < f_{XTAL} ≤ 12 MHz *1	−10°C to +70°C	+5.0V ± 5 %
f_{XTAL} ≤ 10 MHz *1	−10°C to +70°C	+5.0V ± 10 %

CAPACITANCE

(T_a = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_c = 1 MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	$C_{I/O}$				20	pF

DC CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1 *8	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ V_I ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) 0V ≤ V_I ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	+0.45V ≤ V_O ≤ V_{CC}			± 10	μA
V_{TH} Input Current	I_{TH}	V_{TH} = V_{CC}		0.2*2	0.5	mA
V_{DD} Supply Current	I_{DD}			1.5 *2	3.2	mA
V_{CC} Supply Current	I_{CC}			150*2	200	mA

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		83	250	ns
Address Setup to ALE ↓	t_{AL}	*3, *5	65		ns
Address Hold from ALE ↓	t_{LA}	*3, *5	50		ns
Address to $\overline{RD}$ ↓ Delay Time	t_{AR}	*3, *5	150		ns
$\overline{RD}$ ↓ to Address Floating	t_{AFR}	*5		20	ns
Address to Data Input	t_{AD}	*3, *5		360	ns
ALE ↓ to Data Input	t_{LDR}	*3, *5		215	ns
$\overline{RD}$ ↓ to Data Input	t_{RD}	*3, *5		180	ns
ALE ↓ to $\overline{RD}$ ↓ Delay Time	t_{LR}	*3, *5	35		ns
Data Hold Time from $\overline{RD}$ ↑	t_{RDH}	*5	0		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{RL}	*3, *5	115		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read *3, *5	280		ns
		OP Code Fetch *3, *5	530		ns
ALE Width High	t_{LL}	*3, *5	125		ns
$\overline{M1}$ Setup Time to $\overline{ALE}$ ↓	t_{ML}	*3	65		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*3	50		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*3	65		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*3	50		ns
Address to $\overline{WR}$ ↓ Delay	t_{AW}	*3, *5	150		ns
ALE ↓ to Data Output	t_{LDW}	*3, *5		195	ns
$\overline{WR}$ ↓ to Data Output	t_{WD}	*5		100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time	t_{LW}	*3, *5	35		ns
Data Setup Time to $\overline{WR}$ ↑	t_{DW}	*3, *5	230		ns
Data Hold Time from $\overline{WR}$ ↑	t_{WDH}	*3, *5	95		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{WL}	*3, *5	115		ns
$\overline{WR}$ Width Low	t_{WW}	*3, *5	280		ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*6	1		μs
			*7	500		ns
		$\overline{SCK}$ Output		2		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*6	400		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*6	400		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*6		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*6		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*6			210	ns

DC CHARACTERISTICS

(T_a = −40°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1 *8	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ V_I ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3); 0V ≤ V_I ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	+0.45V ≤ V_O ≤ V_{CC}			± 10	μA
V_{TH} Input Current	I_{TH}	V_{TH} = V_{CC}		0.2	0.6	mA
V_{DD} Supply Current	I_{DD}			1.5 *2	3.5	mA
V_{CC} Supply Current	I_{CC}			150*2	220	mA

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		100	250	ns
Address Setup to ALE ↓	t_{AL}	*4, *5	100		ns
Address Hold from ALE ↓	t_{LA}	*4, *5	70		ns
Address to $\overline{RD}$ ↓ Delay Time	t_{AR}	*4, *5	200		ns
$\overline{RD}$ ↓ to Address Floating	t_{AFR}	*5		20	ns
Address to Data Input	t_{AD}	*4, *5		480	ns
ALE ↓ to Data Input	t_{LDR}	*4, *5		300	ns
$\overline{RD}$ ↓ to Data Input	t_{RD}	*4, *5		250	ns
ALE ↓ to $\overline{RD}$ ↓ Delay Time	t_{LR}	*4, *5	50		ns
Data Hold Time from $\overline{RD}$ ↑	t_{RDH}	*5	0		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{RL}	*4, *5	150		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read *4, *5	350		ns
		OP Code Fetch *4, *5	650		ns
ALE Width High	t_{LL}	*4, *5	160		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}	*4	100		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*4	70		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*4	100		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*4	70		ns
Address to $\overline{WR}$ ↓ Delay	t_{AW}	*4, *5	200		ns
ALE ↓ to Data Output	t_{LDW}	*4, *5		210	ns
$\overline{WR}$ ↓ to Data Output	t_{WD}	*5		100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time	t_{LW}	*4, *5	50		ns
Data Setup Time to $\overline{WR}$ ↑	t_{DW}	*4, *5	300		ns
Data Hold Time from $\overline{WR}$ ↑	t_{WDH}	*4, *5	130		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{WL}	*4, *5	150		ns
$\overline{WR}$ Width Low	t_{WW}	*4, *5	350		ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*6	1.2		μs
			*7	500		ns
		$\overline{SCK}$ Output		2.4		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*6	500		ns
			*7	200		ns
		$\overline{SCK}$ Output		1.1		μs
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*6	500		ns
			*7	200		ns
		$\overline{SCK}$ Output		1.1		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*6		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*6		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*6			210	ns

HOLD OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
HOLD ↑ Setup Time to ALE ↑	t_{SHDL}		2T + 150			ns
ALE ↑ to HLDA ↑ Delay	t_{DLHA}				T + 150	ns
HLDA ↑ to BUS Floating	t_{FBHA}		0			ns
HOLD ↓ to HLDA ↓ Delay	t_{HDDA}		T −50		4T + 150	ns
HLDA ↓ to Bus Enable Time	t_{EHAB}		0			ns
Bus Setup Time to ALE	t_{BL}		2T −100			ns

COMPARATOR CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Comparison Accuracy	V_{ACOMP}				± 100	mV
Threshold Voltage	V_{TH}		0		V_{CC}+0.1	V
Comparison Time	t_{COMP}		144		145	T_{CYC}
PT Input Voltage	V_{IPT}		0		V_{CC}	V

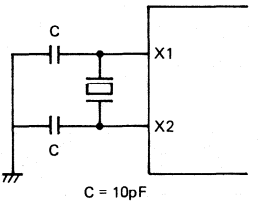
ZERO-CROSS CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

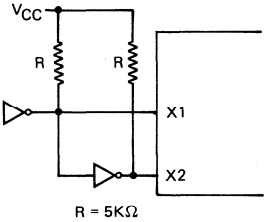
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

*1: XTAL oscillation circuit



C = 10pF

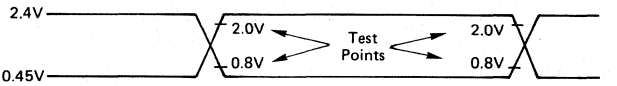
*8: External clock drive circuit



R = 5KΩ

*2: T_a = +25°C, V_{CC} = V_{DD} = 5V
*3: f_{XTAL} = 12 MHz
*4: f_{XTAL} = 10 MHz
*5: Load Capacitance: C_L = 150 pF
*6: Asynchronous mode with 1x baud rate, synchronous, I/O interface mode
*7: Asynchronous mode with 16x or 64x baud rate

AC TIMING TEST POINTS



EXTERNAL CLOCK

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
High Level Width	$t_{\phi H}$		30	250	ns
Low Level Width	$t_{\phi L}$		30	250	ns
Rising Time	t_r		0	30	ns
Falling Time	t_f		0	30	ns

DATA RETENTION CHARACTERISTICS

(T_a = −10 to +70°C, V_{CC} = 0V, V_{DD} = V_{DDDR})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Voltage	V_{DDDR}	RESET = V_{IL}	3.2		5.5	V
Data Retention Supply Current	I_{DDDR}	RESET = V_{IL}, V_{DDDR} = 3.2 V		1.3	3.0	mA

BUS TIMING DEPENDING ON t_{CYC}

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNITS
t_{AL}	2T − 100	MIN	ns
t_{LA}	T − 30	MIN	ns
t_{AR}	3T − 100	MIN	ns
t_{AD}	7T − 220 *1	MAX	ns
t_{LDR}	5T − 200 *1	MAX	ns
t_{RD}	4T − 150 *1	MAX	ns
t_{LR}	T − 50	MIN	ns
t_{RL}	2T − 50	MIN	ns
t_{RR}	4T − 50 (Data Read) *1 7T − 50 (OP Code Fetch) *1	MIN	ns
t_{LL}	2T − 40	MIN	ns
t_{ML}	2T − 100	MIN	ns
t_{LM}	T − 30	MIN	ns
t_{IL}	2T − 100	MIN	ns
t_{LI}	T − 30	MIN	ns
t_{AW}	3T − 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T − 50	MIN	ns
t_{DW}	4T − 100 *1	MIN	ns
t_{WDH}	2T − 70	MIN	ns
t_{WL}	2T − 50	MIN	ns
t_{WW}	4T − 50 *1	MIN	ns
t_{CYK}	12T ($\overline{SCK}$ Input) *2 24T ($\overline{SCK}$ Output)	MIN	ns
t_{KKL}	5T + 5 (SCK Input) *2 12T − 100 ($\overline{SCK}$ Output)	MIN	ns
t_{KKH}	5T + 5 ($\overline{SCK}$ Input) *2 12T − 100 ($\overline{SCK}$ Output)	MIN	ns

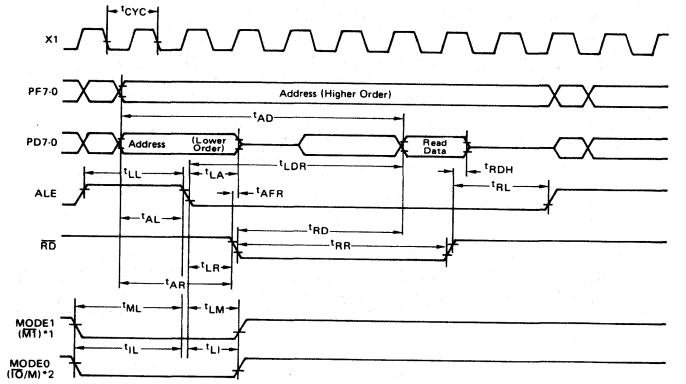
*1: Add 3T to each parameter in the case of external memory access using program WAIT function.

*2: Asynchronous mode with 1x baud rate, Synchronous, I/O Interface Mode

*3: T = t_{CYC} = 1/f_{XTAL}

*4: The items out of this table are not dependent on f_{XTAL}.

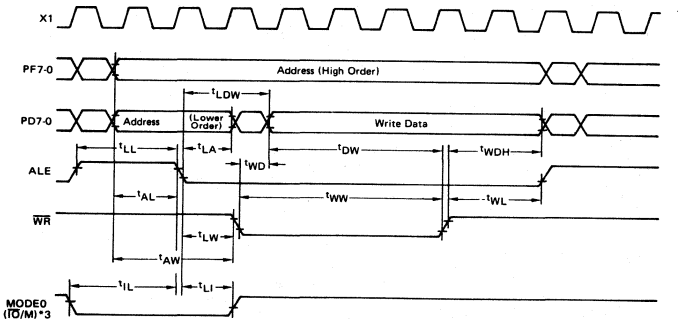
READ OPERATION



*1: $\overline{M1}$ signal is output to the MODE1 pin at 1st OP code fetch cycle when MODE 1 pin is pulled-up to V_{CC}.

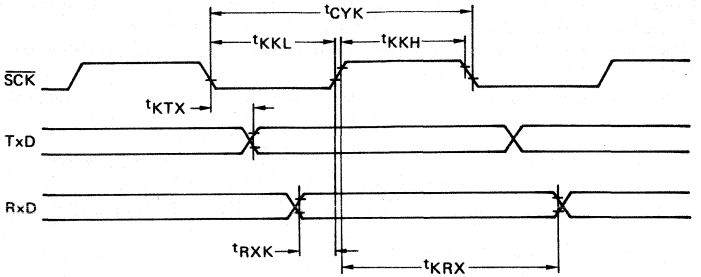
*2: $\overline{IO}/M$ signal is output to the MODE0 pin at sr to sr2 register read timing when MODE0 pin is pulled-up to V_{CC}.

WRITE OPERATION

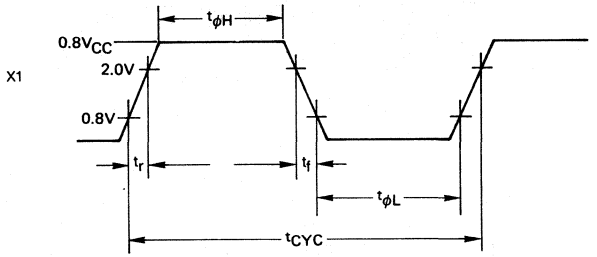


*3: $\overline{IO}/M$ signal is output to the MODE0 pin at sr to sr2 register write timing when MODE0 pin is pulled-up to V_{CC}.

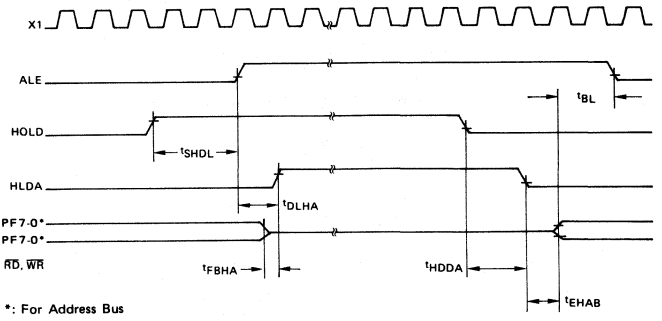
SERIAL OPERATION



X1 INPUT WAVEFORM

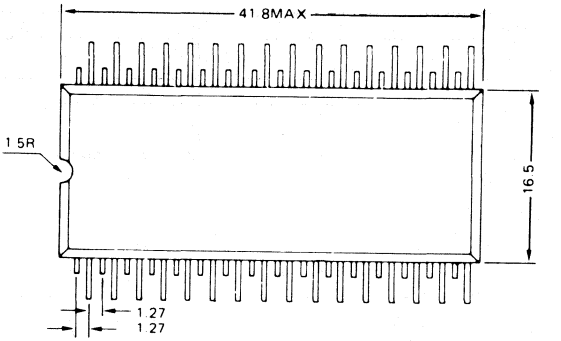


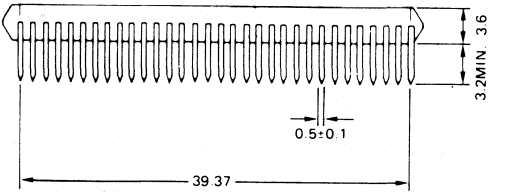
HOLD OPERATION



*: For Address Bus

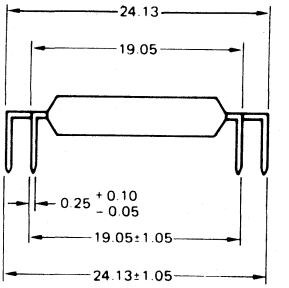
64 PIN PLASTIC
QUIP OUTLINE BENT LEADS
(Unit : mm)
μPD7809G



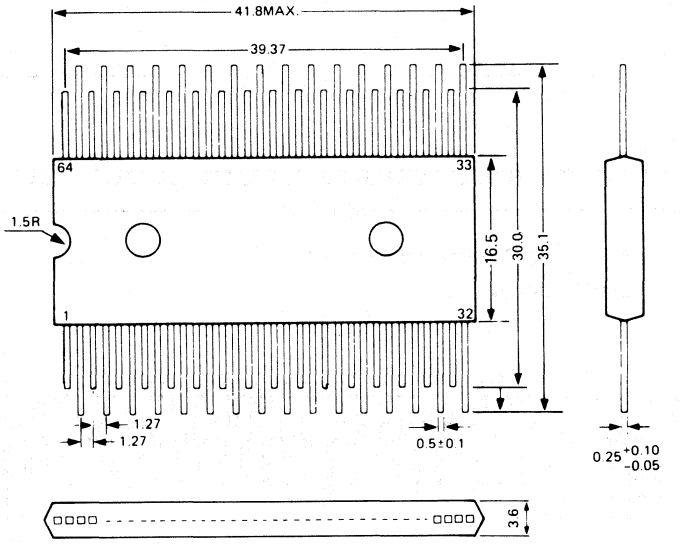


When ordering this package, specify as follows:

μPD7809G-xxx-36



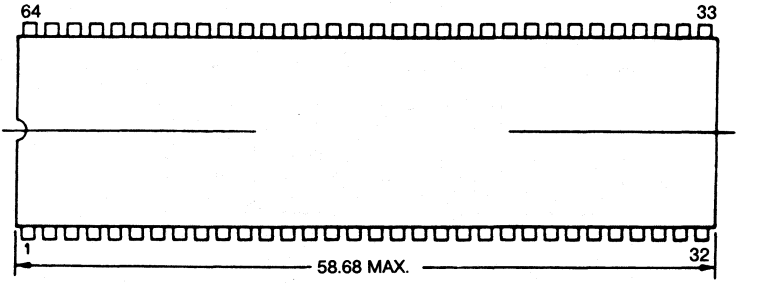
64 PIN PLASTIC
PACKAGE OUTLINE
STRAIGHT LEADS
(Unit : mm)
μPD7809



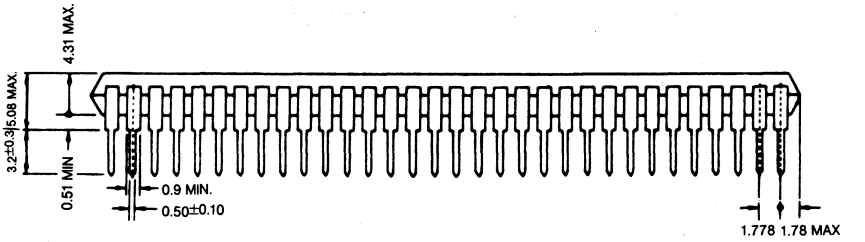
When ordering this package, specify as follows: μPD7809G-xxx-37

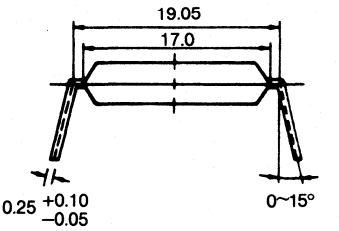
PACKAGE OUTLINE
μPD7809CW

64-PIN SHRINK DIP



When ordering this package, specify as follows:
μPD7807CW
μPD7808CW-xxx





ELECTRICAL SPECIFICATIONS
AND PACKAGE OUTLINES FOR
μPD78P09

ABSOLUTE MAXIMUM RATINGS

(T_a = 25° C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNITS
Power Supply Voltage	V_{CC}		−0.5 to +7.0	V
	V_{DD}		−0.5 to +7.0	V
Input Voltage	V_I		−0.5 to +7.0	V
Output Voltage	V_O		−0.5 to + 7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−0.5	mA
		All Output Pin Total	−20	mA
Threshold Voltage	V_{TH}		-0.5 to V_{CC} + 0.1	V
Operating Temperature	T_{opt}	4 MHz < f_{XTAL} ≤ 12 MHz	−10 to +50	°C
Storage Temperature	T_{stg}		−65 to +150	°C

OPERATING CONDITION

PARAMETER / OSC. FREQ.	T_a	V_{CC}, AV_{CC}
4 MHz ≤ f_{XTAL} ≤ 12 MHz	−10°C to +70°C	+5.0V ± 5 %

CAPACITANCE

(T_a = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_C = 1 MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	$C_{I/O}$				20	pF

DC CHARACTERISTICS

(T_a = −10°C to +50°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1 *8	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ V_I ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) 0V ≤ V_I ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	+0.45V ≤ V_O ≤V_{CC}			± 10	μA
V_{TH} Input Current	I_{TH}	V_{TH} = V_{CC}		0.2*2	0.5	mA
V_{DD} Supply Current	I_{DD}			1.5 *2	3.2	mA
V_{CC} Supply Current	I_{CC}			240*2	320	mA

AC CHARACTERISTICS
READ/WRITE OPERATION

(T_a = −10°C to +50°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		83	250	ns
Address Setup to ALE ↓	t_{AL}	*3, *5	65		ns
Address Hold from ALE ↓	t_{LA}	*3, *5	50		ns
Address to $\overline{RD}$ ↓ Delay Time	t_{AR}	*3, *5	150		ns
$\overline{RD}$ ↓ to Address Floating	t_{AFR}	*5		20	ns
Address to Data Input	t_{AD}	*3, *5		360	ns
ALE ↓ to Data Input	t_{LDR}	*3, *5		215	ns
$\overline{RD}$ ↓ to Data Input	t_{RD}	*3, *5		180	ns
ALE ↓ to $\overline{RD}$ ↓ Delay Time	t_{LR}	*3, *5	35		ns
Data Hold Time from $\overline{RD}$ ↑	t_{RDH}	*5	0		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{RL}	*3, *5	115		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read *3, *5	280		ns
		OP Code Fetch *3, *5	530		ns
ALE Width High	t_{LL}	*3, *5	125		ns
$\overline{M1}$ Setup Time to $\overline{ALE}$ ↓	t_{ML}	*3	65		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*3	50		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*3	65		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*3	50		ns
Address to $\overline{WR}$ ↓ Delay	t_{AW}	*3, *5	150		ns
ALE ↓ to Data Output	t_{LDW}	*3, *5		195	ns
$\overline{WR}$ ↓ to Data Output	t_{WD}	*5		100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time	t_{LW}	*3, *5	35		ns
Data Setup Time to $\overline{WR}$ ↑	t_{DW}	*3, *5	230		ns
Data Hold Time from $\overline{WR}$ ↑	t_{WDH}	*3, *5	95		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{WL}	*3, *5	115		ns
$\overline{WR}$ Width Low	t_{WW}	*3, *5	280		ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*6	1.66		μs
			*7	500		ns
		$\overline{SCK}$ Output		2		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*6	750		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*6	750		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*6		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*6		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*6			210	ns

HOLD OPERATION

(T_a = −10°C to +50°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
HOLD ↑ Setup Time to ALE ↑	t_{SHDL}		2T + 150			ns
ALE ↑ to HLDA ↑ Delay	t_{DLHA}				T + 150	ns
HLDA ↑ to BUS Floating	t_{FBHA}		0			ns
HOLD ↓ to HLDA ↓ Delay	t_{HDDA}		T −50		4T + 150	ns
HLDA ↓ to Bus Enable Time	t_{EHAB}		0			ns
Bus Setup Time to ALE	t_{BL}		2T −100			ns

(T_a = −10°C to +50°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

COMPARATOR CHARACTERISTICS

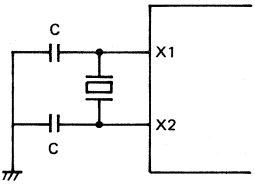
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Comparison Accuracy	V_{ACOMP}				± 100	mV
Threshold Voltage	V_{TH}		0		V_{CC}+0.1	V
Comparison Time	t_{COMP}		144		145	T_{CYC}
PT Input Voltage	V_{IPT}		0		V_{CC}	V

(T_a = −10°C to +50°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

ZERO-CROSS CHARACTERISTICS

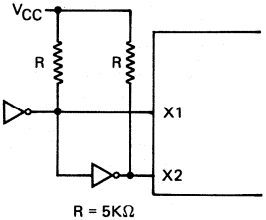
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

*1: XTAL oscillation circuit



C = 10pF

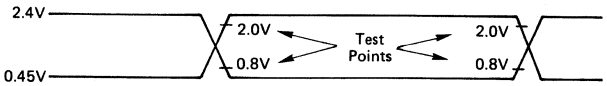
*8: External clock drive circuit



R = 5KΩ

*2: T_a = +25°C, V_{CC} = V_{DD} = 5V
*3: f_{XTAL} = 12 MHz
*4: f_{XTAL} = 10 MHz
*5: Load Capacitance: C_L = 150 pF
*6: Asynchronous mode with 1x baud rate, synchronous, I/O interface mode
*7: Asynchronous mode with 16x or 64x baud rate

AC TIMING TEST POINTS



EXTERNAL CLOCK

(T_a = −10°C to +50°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
High Level Width	$t_{\phi H}$		30	250	ns
Low Level Width	$t_{\phi L}$		30	250	ns
Rising Time	t_r		0	30	ns
Falling Time	t_f		0	30	ns

DATA RETENTION CHARACTERISTICS

(T_a = −10 to +50°C, V_{CC} = 0V, V_{DD} = V_{DDDR})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Voltage	V_{DDDR}	RESET = V_{IL}	3.2		5.5	V
Data Retention Supply Current	I_{DDDR}	RESET = V_{IL}, V_{DDDR} = 3.2 V		1.3	3.0	mA

BUS TIMING DEPENDING ON t_{CYC}

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNITS
t_{AL}	2T − 100	MIN	ns
t_{LA}	T − 30	MIN	ns
t_{AR}	3T − 100	MIN	ns
t_{AD}	7T − 220 *1	MAX	ns
t_{LDR}	5T − 200 *1	MAX	ns
t_{RD}	4T − 150 *1	MAX	ns
t_{LR}	T − 50	MIN	ns
t_{RL}	2T − 50	MIN	ns
t_{RR}	4T − 50 (Data Read) *1 7T − 50 (OP Code Fetch) *1	MIN	ns
t_{LL}	2T − 40	MIN	ns
t_{ML}	2T − 100	MIN	ns
t_{LM}	T − 30	MIN	ns
t_{IL}	2T − 100	MIN	ns
t_{LI}	T − 30	MIN	ns
t_{AW}	3T − 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T − 50	MIN	ns
t_{DW}	4T − 100 *1	MIN	ns
t_{WDH}	2T − 70	MIN	ns
t_{WL}	2T − 50	MIN	ns
t_{WW}	4T − 50 *1	MIN	ns
t_{CYK}	20T (SCK Input) *2 24T (SCK Output)	MIN	ns
t_{KKL}	10T − 80 (SCK Input) *2 12T − 100 (SCK Output)	MIN	ns
t_{KKH}	10T − 80 (SCK Input) *2 12T − 100 (SCK Output)	MIN	ns

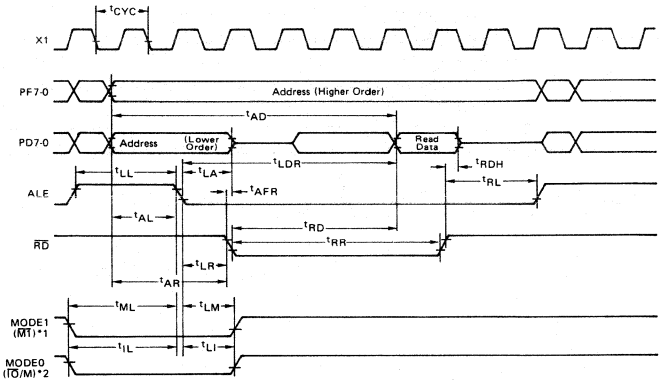
*1: Add 3T to each parameter in the case of external memory access using program WAIT function.

*2: Asynchronous mode with 1x baud rate, Synchronous, I/O Interface Mode

*3: T = t_{CYC} = 1/f_{XTAL}

*4: The items out of this table are not dependent on f_{XTAL}.

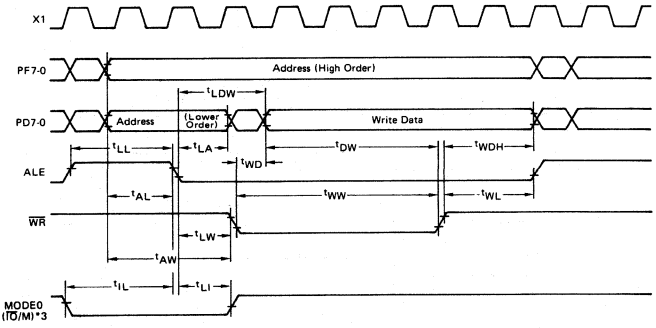
READ OPERATION



*1: $\overline{M1}$ signal is output to the MODE1 pin at 1st OP code fetch cycle when MODE 1 pin is pulled-up to V_{CC}.

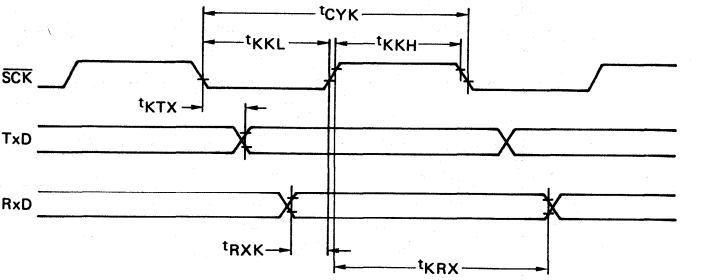
*2: $\overline{IO}$/M signal is output to the MODE0 pin at sr to sr2 register read timing when MODE0 pin is pulled-up to V_{CC}.

WRITE OPERATION

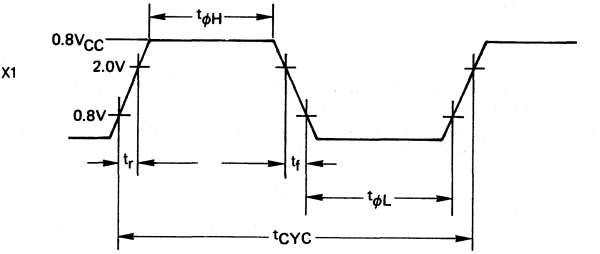


*3: $\overline{IO}$/M signal is output to the MODE0 pin at sr to sr2 register write timing when MODE0 pin is pulled-up to V_{CC}.

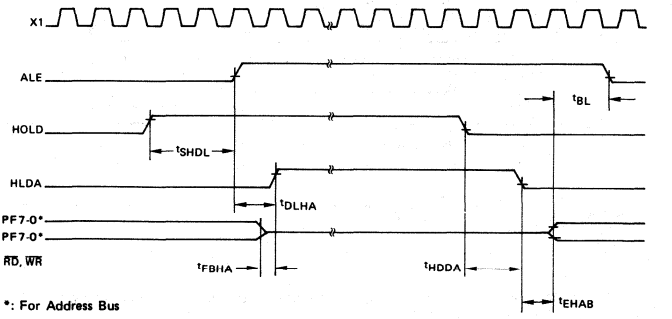
SERIAL OPERATION



X1 INPUT WAVEFORM



HOLD OPERATION



DC PROGRAMMING CHARACTERISTICS

(T_a = +25°C ± 5°C, V_{CC} = +5V ± 10 %, V_{PP} = +21V ± 0.5V, V_{SS} = 0V, V_{CC} −0.8 ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current All except INT1, TI(PC3)	I_{LI}	0V ≤ V_{IN} < V_{CC}			± 10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = −200μA	2.4			V
V_{CC} Supply Current	I_{CC}			200	300	mA
Input Low Level (All Inputs)	V_{IL}		0		0.8	V
Input High Level	V_{IH1}	All except $\overline{SCK}$, RESET and X1	2.0		V_{CC}	V
	V_{IH2}	SCK, X1	0.8 V_{CC}		V_{CC}	V
V_{PP} Supply Current	I_{PP}	$\overline{PGM}$ = V_{IL}			30	mA

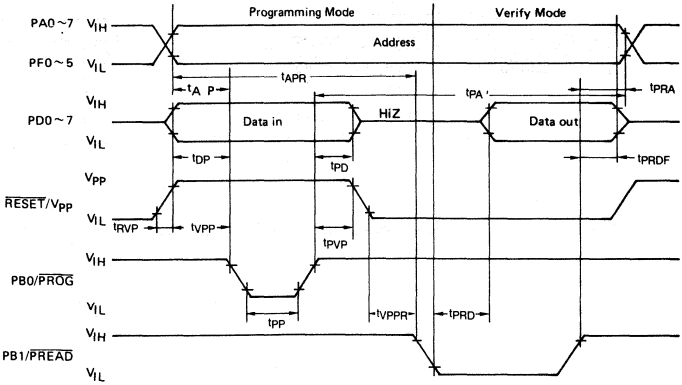
AC PROGRAMMING CHARACTERISTICS

(T_a = +25°C ± 5°C, V_{CC} = +5V ± 10 %, V_{PP} = +21V ± 0.5V, V_{SS} = 0V, V_{CC} −0.8 ≤ V_{DD} ≤ V_{CC})

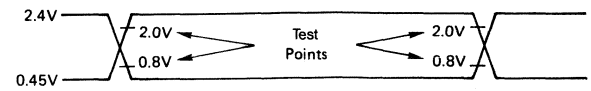
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Address Setup Time	Programming Mode	t_{AP}		2			μs
	Verify Mode	t_{APR}		2			μs
V_{PP} Setup Time		t_{VPP}		2			μs
Data Setup Time		t_{DP}		2			μs
Address Hold Time	Programming Mode	t_{PA}		2			μs
	Verify Mode	t_{PRA}		0			μs
V_{PP} Hold Time		t_{PVP}		2			μs
Data Hold Time		t_{PD}		2			μs
$\overline{PREAD}$ to Output Float Delay		t_{PRDR}		0		130	ns
Data Valid from $\overline{PREAD}$		t_{PRD}				1	μs
$\overline{PROG}$ Pulse Width During Programming		t_{PP}		45	50	55	ms
V_{PP} Pulse Rise Time During Programming		t_{RVP}		50			ns
V_{PP} Recovery Time		t_{VPPR}		2			μs
Input Rise/Fall Time		t_{IR}, t_{IF}				20	ns

TIMING WAVEFORM

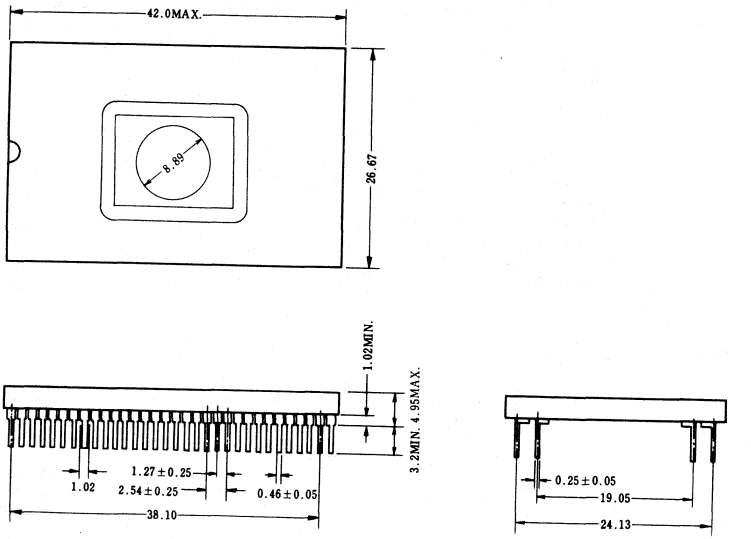
PROGRAMMING



AC TIMING MEASUREMENT POINTS



64 PIN CERAMIC QUIP OUTLINE (Unit : mm)
μPD78P09R



Note: The μPD78P09 is programmable on NEC programmer PG 1000 together with programmer module PG 1003.

HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH ON CHIP A/D CONVERTER

DESCRIPTION

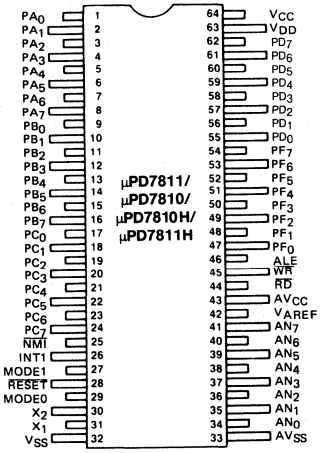
The NEC μPD7810/7811 is a high-performance single-chip microcomputer integrating sophisticated on-chip peripheral functionality normally provided by external components. The devices's internal 16-bit ALU and data paths, combined with a powerful instruction set and addressing, make the μPD7810/7811 appropriate in data processing as well as control applications. The device integrates a 16-bit ALU, 4K-ROM, 256-byte RAM with an 8-channel A/D converter, a multifunction 16-bit timer/event counter, two 8-bit timers, a USART and two zero-cross detect inputs on a single die, to direct the device into fast, high-end processing applications involving analog signal interface and processing.

The μPD7811 is the mask-ROM high volume production device embedded with customer program. The μPD7810 is a ROM-less version for prototyping and small volume production. The μPD78PG11E is a piggy-back EPROM version for design development.
The μPD7810H/11H is a high speed version of the μPD7810/11 (15 MHz operation)

FEATURES

- Powerful Instruction Set Including 16-bit Multiply and Divide, 158 instructions
- High-Speed 1μsec Cycle Time-12 MHz Operation (0.85 μsec for 7810H/11H, 15 MHz)
- On-Chip 4K-Byte ROM (7811), 256-Byte RAM
- 44 I/O Lines
- Easily Expandable Memory up to 60K Bytes (externally)
- On-Chip 8-Bit A/D Converter-8 Input Channels
- Multi-Functional 16-Bit Timer/Counter
- Two Programmable 8-Bit Timers
- Full-Duplex Serial Communication Interface, synchronous and asynchronous
- Zero-Cross Detection Capability
- Vectored Interrupts, 3 external/8 internal
- Low Power Standby Operation
- 8085A Bus Compatible
- Single Power Supply +5V, N-MOS Technology
- Available in 64 Pin Package
- Standby function
- On-chip clock generator
- 64K-Byte total memory address range

PIN CONFIGURATION



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION	
1–8	PA_0–PA_7	Port A: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port A in input mode.	
9–16	PB_0–PB_7	Port B: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port B in input mode.	
17	PC_0	Port C: (Three-state input/output) 8-bit programmable I/O port. Each line independently pro-programmable as an input or output. Alternatively, Port C may be used as control lines for USART and timer, event-counter and external interrupts. Reset puts Port C in Port mode and all lines in input mode.	Transmit Data (TxD): Serial data output terminal.
18	PC_1		Receive Data (RxD): Serial data input terminal.
19	PC_2		Serial Clock ($\overline{SCK}$): Serial clock input/output terminal. When internal clock is used, the output can be selected; when an external clock is used, the input can be selected.
20	PC_3		Timer Input ((TI)/interrupt request input (INT2): Timer clock input terminal; can also be used as falling edge, maskable-interrupt input terminal and AC input zero-cross detection terminal.
21	PC_4		Timer Output (TO): This output signal is a square wave whose frequency is determined by the timer/counter.
22	PC_5		Counter Input (CI): External pulse input terminal to the timer/event counter.
23–24	PC_6, PC_7		Counter Outputs 0, 1 (CO_0–CO_1): Programmable rectangular wave output terminal based on timer/event counter.
25	$\overline{NMI}$	Falling-edge, nonmaskable interrupt ($\overline{NMI}$) input.	
26	INT1	This signal is a rising-edge, maskable interrupt input. This input is also used to make the zero-cross detection AC input.	
27	MODE1	Used as input in conjunction with MODE0 to select appropriate memory expansion mode. Also outputs M1 Signal during each opcode fetch.	
28	$\overline{RESET}$	(Input, active low), $\overline{RESET}$ initializes the μPD7811.	
29	MODE0	Used as input in conjunction with MODE1 to select appropriate memory expansion mode. Also used to output $\overline{IO}$/M.	
30–31	X_2, X_1 (crystal)	This is a crystal connection terminal for system clock oscillation. When an external clock is supplied X_1 is the input.	
32	V_{SS}	Power supply ground potential.	
33	AV_{SS}	A/D converter power supply ground potential. Sets conversion's range lower limit.	

PIN IDENTIFICATION (cont.)

PIN NO.	PIN SYMBOL	FUNCTION
34–41	AN_0–AN_7	Eight analog inputs to the A/D converter. AN_7–AN_4 can also be used as a digital input port for falling edge detection.
42	V_{AREF}	Reference voltage for A/D converter. Sets conversion's range upper limit.
43	AV_{CC}	Power supply voltage for A/D converter.
44	$\overline{RD}$	(Three-state output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes high during Reset.
45	$\overline{WR}$	(Three-state output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes high during Reset.
46	ALE	The strobe signal is for latching the address signal to the output from PD_7–PD_0 when accessing external expansion memory.
47–54	PF_0–PF_7	Port F: (Three-state input/output) 8-bit programmable I/O port. Each line configurable independently as an input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
55–62	DB_0–DB_7	Port D: 8-bit programmable I/O port. This byte can be designated as either input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
63	V_{DD}	This ia a second power supply line for on-chip RAM back-up
64	V_{CC}	+5V power supply.

Notes: 1 clock cycle = 1 CL = 3/f.
1 machine cycle = 3 or 4 clock cycles.
1 instruction cycle = 1 to 19 machine cycles.
f: System clock frequency (MHz).

NEW INSTRUCTIONS

In addition to the existing instruction set for μPD7801, the following new instructions are incorporated in the μPD7810/11:

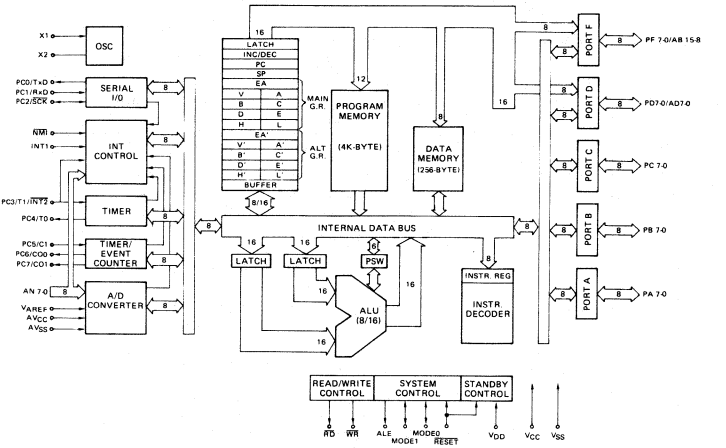
16-bit data transfer between memory and extended accumulator
16-bit data arithmetic and logical operation.

16-bit data addition and subtraction and 16-bit comparsion.
16-bit data shift and rotation
direct multiply and divide instructions.

8-bit by 8-bit division less then 8 μsec execution time.

16-bit divided by 8-bit less than 15 μsec execution
table look-up operation.
Register pair HL and DE are used as base register. Accumulator, B-register and extended accumulator are used as index register.

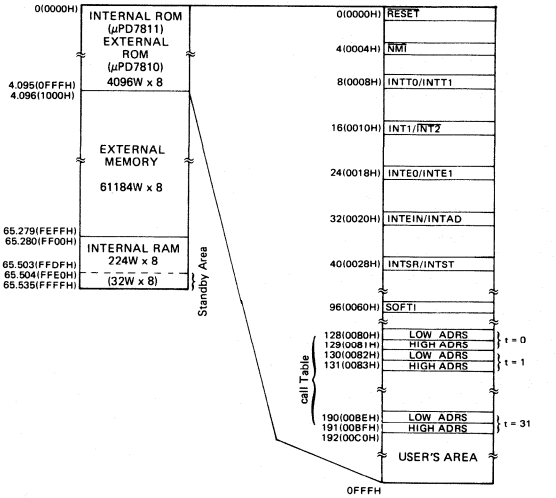
BLOCK DIAGRAM



Note: the μPD7810/10H has no programmable ROM (4K bytes) on chip.

MEMORY MAP

The μPD7811 can directly address up to 64K-bytes of memory. Except for the on-chip ROM (0-4095) and RAM (65280–65535), any memory location can be used as ROM or RAM. The following memory map defines the 0-64K-byte memory space for the μPD7811.



INPUT/OUTPUT

8 Analog Input Lines
44 Digital I/O Lines: five 8-bit ports (Port A, Port B, Port C, Port D, Port F) and 4 input lines (AN_4–AN_7)

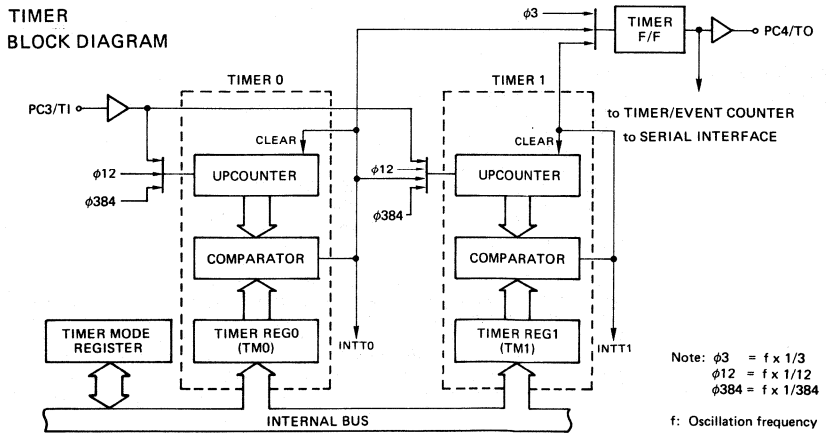
1. Analog Input Lines
   AN_0–AN_7 are configured as analog input lines for on-chip A/D converter.
2. Port Operation
   - Port A, Port B, Port C, Port F
     Each line of these ports can be individually programmed as an input or as an output. When used as I/O ports, all have latches outputs, high-impedance inputs.
   - Port D
     Port D can be programmed as a byte input or a byte output.
   - AN_4–AN_7
     The high-order analog input lines, AN_4–AN_7 can be used as digital input lines for falling edge detection.
3. Control Lines
   Under software control, each line of Port C can be configured individually to provide control lines for serial interface, timer and timer/counter, and interrupts.
4. Memory Expansion
   In addition to the single-chip operation mode the μPD7811 has 4 memory expansion modes. Under software control, Port D can provide multiplexed low-order address and data bus and Port F can provide high-order address bus. The relation between memory expansion modes and the pin configurations of Port D and Port F is shown in the table that follows.

MEMORY EXPANSION		PORT CONFIGURATION
None	Port D Port F	I/O Port I/O Port
256 Bytes	Port D Port F	Multiplexed Address/Data Bus I/O Port
4K Bytes	Port D Port F_0–F_3 Port F_4–F_7	Multiplexed Address/Data Bus Address Bus I/O Port
16K Bytes	Port D Port F_0–F_5 Port F_6–F_7	Multiplexed/Data Bus Address Bus I/O Port
60K Bytes	Port D Port F	Multiplexed Address/Data Bus Address Bus

TIMERS

The timer/event counter consists of two 8-bit timers. The timers may be programmed independently or may be cascaded and used as a 16-bit timer. The timer can be set by software to increment at intervals of 4 machine cycles (1μs at 12MHz operation) or 128 machine cycles (32μs at 12MHz), or to increment on receipt of a pulse at TI.

TIMER BLOCK DIAGRAM



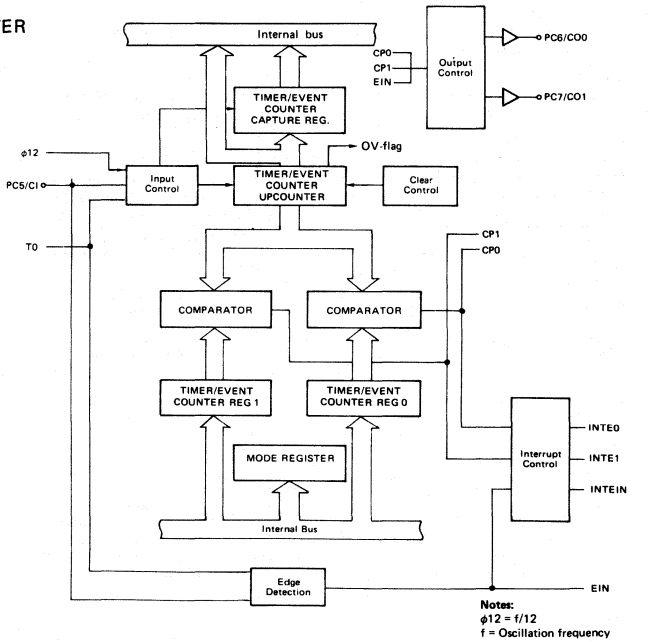
FUNCTIONAL DESCRIPTION (CONT.)

TIMER/EVENT COUNTER

The 16-bit Multifunctional timer/event counter can be used for the following operations:

- Interval timer
- External event counter
- Frequency measurement
- Pulse width measurement
- Programmable square-wave output
- Single pulse generation

TIMER/EVENT COUNTER BLOCK DIAGRAM



ANALOG/DIGITAL CONVERTER

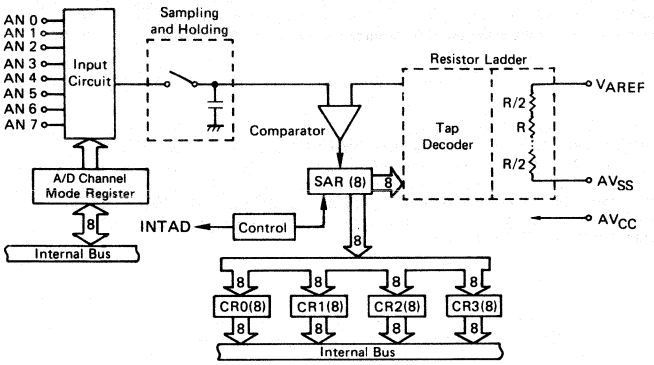
- 8 Input Channels
- 4 Conversion Result Registers
- 2 Powerful Operation Modes
  - Auto Scan Mode
  - Channel Select Mode
- Successive Approximation Technique

Absolute Accuracy	± 1.5 LSB (± 0.6%)
Conversion Range	0 ~ 5V
Conversion Time	48 μs

- Interrupt Generation

The μPD7810/7811 features an 8-bit, high-speed, high accuracy A/D converter. The A/D converter comprises a 256-Resistor Ladder and Successive Approximation Register (SAR). There are four conversion result registers (CR_0–CR_3). The 8-channel analog input may be operated in either of two modes. In the select mode, the conversion value of one analog input is sequentially stored in CR_0–CR_3. In the scan mode, the upper four channels or the lower four channels may be specified. Then those four channels will be consecutively selected and the conversion results stored sequentially in the four conversion result registers.

A/D CONVERTER BLOCK DIAGRAM

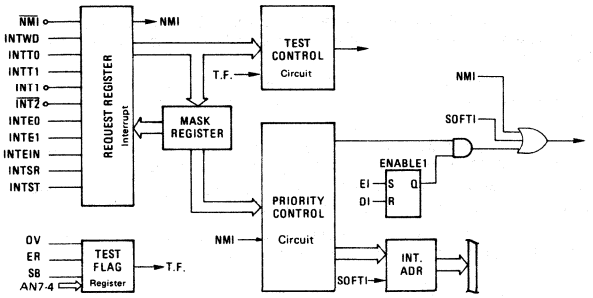


INTERRUPT STRUCTURE

There are 11 interrupt sources. Three are external interrupts and 8 are internal. These 11 interrupt sources are divided into 6 priority levels as shown in the table below.

INTERRUPT REQUEST	INTERRUPT VECTOR	TYPE OF INTERRUPT		IN/EXT
IRQ0	4	NMI	(Non-maskable interrupt)	External
IRQ1	8	INTT0 INTT1	(Coincidence signal from timer 0) (Coincidence signal from timer 1)	Internal
IRQ2	16	INT1 INT2	(Maskable intrrupt) (Maskable interrupr)	External
IRQ3	24	INTE0 INTE1	(Coincidence signal from timer/ event counter) Coincidence signal from timer/ event counter)	Internal
IRQ4	32	INTEIN INTAD	(Falling signal of C1 and T0 counter) (A/D converter interrupt)	In/External
IRQ5	40	INTSR INST	(Serial receive interrupt) (Serial send interrupt)	Internal

INTERRUPT CONTROL BLOCK DIAGRAM



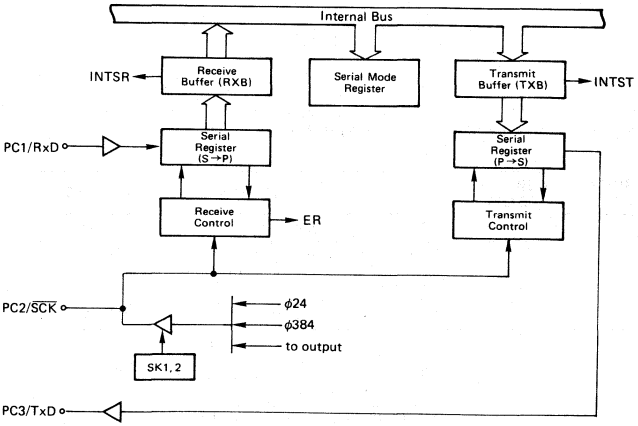
STANDBY FUNCTION

The μPD7810/7811 offers a standby function that allows the user to save up to 32 bytes of RAM with backup power (V_{DD}) if the main power (V_{CC}) fails. On powerup the μPD7811 checks whether recovery was made from standby mode or from cold start.

UNIVERSAL SERIAL INTERFACE

The serial interface can operate in any of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first for ease of communication with certain peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception. In the search mode, data are transferred one bit at a time from serial register to receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from serial register to transmit buffer occurs 8 bits at a time.

UNIVERSAL SERIAL INTERFACE BLOCK DIAGRAM



Note: $\phi 24 = \frac{1}{24}$

f: oscillation frequency (MHz)

$\phi 384 = \frac{1}{384}$

ZERO-CROSSING DETECTOR

The INT1 and INT2 terminals (used also as TI and PC_3) can be used to detect the zero-crossing point of slow moving AC signals. When driven directly, these pins respond as a normal digital input.

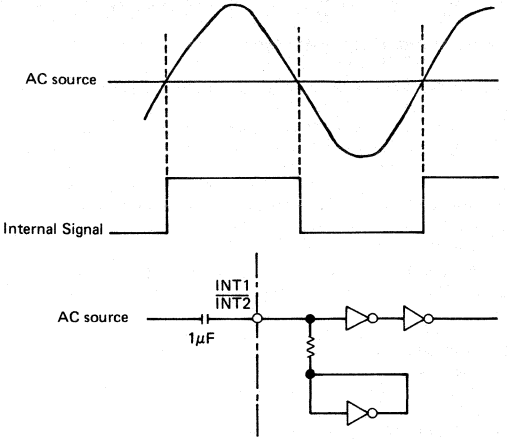
To utilize the zero-cross detection mode, an AC signal of approximately 1 – 1.8V peak-to-peak magnitude and a maximum frequency of 1kHz is coupled through an external capacitor to these pins.

For the INT1 pin, the internal digital state is sensed as a zero until the rising edge crosses the DC average level, when it becomes a one and INT1 interrupt is generated.

For the INT2 pin, the state is sensed as a one until the falling edge crosses the DC average level, when it becomes a zero and INT2 interrupt is generated.

The zero-cross detection capability allows the user to make the 50–60Hz power signal the basis for system timing and to control voltage phase sensitive devices.

ZERO-CROSSING
DETECTION CIRCUIT



MODE0/MODE1-TERMINALS

The logic level applied to M0/M1-Terminals determines the memory map of μPD7810/7811 and the use of Port D/F as multiplexed Address/Data Bus.

M0	M1	MEMORY	ADDRESSES	LOCATION
0	1	4K	0 . . . . . FFFH	internal*
0	0	4K	0 . . . . . FFFH	external
0	1	16K	0 . . . . . .3FFFH	external
1	0	64K	0 . . . . . FEFFH	external

* MO, M1 = 0,1 realizes the ROM version (access of internal ROM), all others represent access of external memory only. In case external memory is used in addition to internal, memory mapping register has to be programmed then (see below).

(using μPD7811)

MEMORY EXPANDES MODES	MEMORY MAPPING REGISTER			NUMBER OF I/O LINES
	MM2	MM1	MM0	
Port Mode	0	0	X	44
256 Expanded	0	1	0	36
4K Expanded	1	0	0	32
16K Expanded	1	1	0	30
60K Expanded	1	1	1	28

HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH ON CHIP A/D CONVERTER

DESCRIPTION

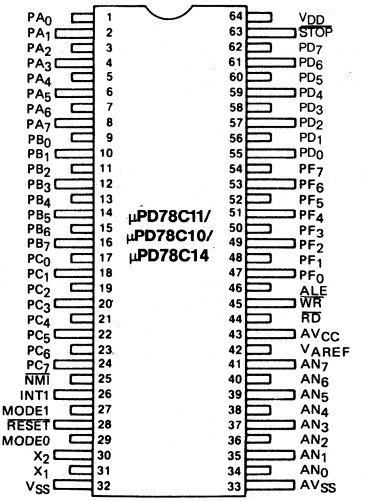
The NEC μPD78C10/C11/C14 is the CMOS version of the μPD7810/11 respectively.
The NEC μPD78C10/C11/C14 is a high-performance single-chip microcomputer integrating sophisticated on-chip peripheral functionality normally provided by external components. The devices's internal 16-bit ALU and data paths, combined with a powerful instruction set and addressing, make up μPD78C10/C11/C14 appropriate in data processing as well as control applications. The device integrates a 16-bit ALU, 4K-ROM, 256-byte RAM with an 8-channel A/D converter, a multifunction 16-bit timer/event counter, two 8-bit timers, a USART and two zero-cross detect inputs on a single die, to direct the device into fast, high-end processing applications involving analog signal interface and processing.

The μPD78C11/C14 are the mask-ROM high volume production devices embedded with customer program. The μPD78C10 is a ROM-less version for prototyping and small volume production.

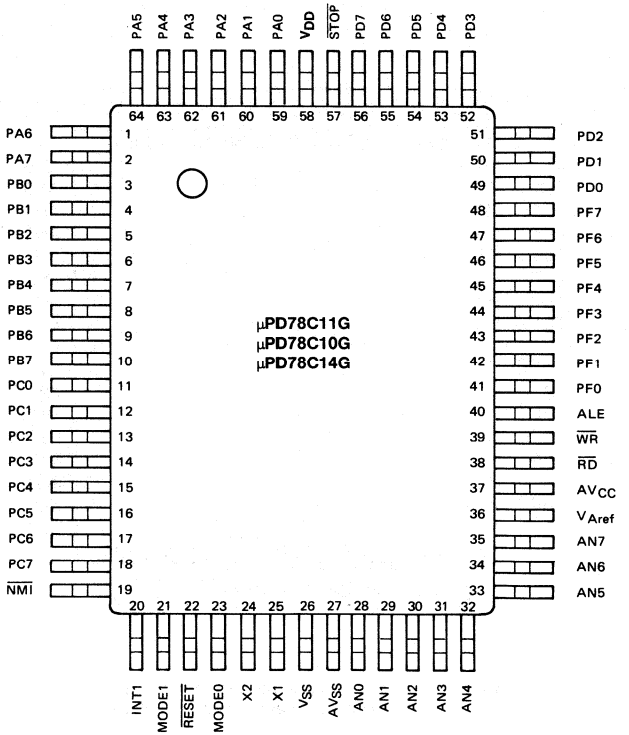
FEATURES

- Powerful Instruction Set Including 16-bit Multiply and Divide, 158 instructions
- High-Speed 1 μsec Cycle Time-12 MHz Operation
- On-Chip 4K-Byte ROM (78C11), 16K-Byte ROM (78C14), 256-Byte RAM
- 44 I/O Lines
- Easily Expandable Memory up to 60K Bytes/48K Bytes (externally)
- On-Chip 8-Bit A/D Converter-8 Input Channels
- Multi-Functional 16-Bit Timer/Counter
- Two Programmable 8-Bit Timers
- Full-Duplex Serial Communication Interface, synchronous and asynchronous
- Zero-Cross Detection Capability
- Vectored Interrupts, 3 external/8 internal
- Low Power Standby Operation
- 8085A Bus Compatible
- Singel Power Supply +5V, CMOS Technology
- Available in 64 Pin/68 Pin Packages (QUIL, FLAT, SHRINK DIP, PLCC)
- Standby functions
- On-chip clock generator
- 64K-Byte total memory address range

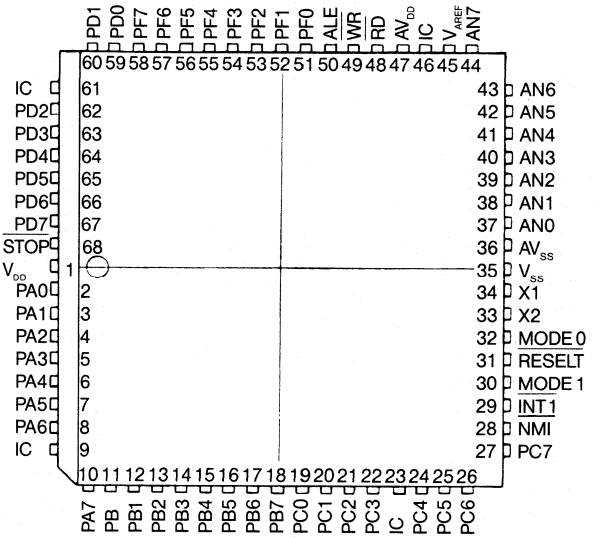
PIN CONFIGURATION QUIL, SHRINK DIP



PIN CONFIGURATION FLAT PACKAGE



PIN CONFIGURATION
68-PIN PLCC PACKAGE



Note: IC = keep this pin open because of internal connection (external connection prohibited)

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION	
1–8	PA_0–PA_7	Port A: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port A in input mode.	
9–16	PB_0–PB_7	Port B: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port B in input mode.	
17	PC_0	Port C: (Three-state input/output) 8-bit programmable I/O port. Each line independently pro-programmable as an input or output. Alternatively, Port C may be used as control lines for USART and timer, event-counter and external interrupts. Reset puts Port C in Port mode and all lines in input mode.	Transmit Data (TxD): Serial data output terminal.
18	PC_1		Receive Data (RxD): Serial data input terminal.
19	PC_2		Serial Clock ($\overline{SCK}$): Serial clock input/output terminal. When internal clock is used, the output can be selected; when an external clock is used, the input can be selected.
20	PC_3		Timer Input ((TI)/interrupt request input (INT2): Timer clock input terminal; can also be used as falling edge, maskable-interrupt input terminal and AC input zero-cross detection terminal.
21	PC_4		Timer Output (TO): This output signal is a square wave whose frequency is determined by the timer/counter.
22	PC_5		Counter Input (CI): External pulse input terminal to the timer/event counter.
23–24	PC_6, PC_7		Counter Outputs 0, 1 (CO_0–CO_1): Programmable rectangular wave output terminal based on timer/event counter.
25	$\overline{NMI}$	Falling-edge, nonmaskable interrupt ($\overline{NMI}$) input.	
26	INT1	This signal is a rising-edge, maskable interrupt input. This input is also used to make the zero-cross detection AC input.	
27	MODE1	Used as input in conjunction with MODE0 to select appropriate memory expansion mode. Also outputs M1 Signal during each opcode fetch.	
28	$\overline{RESET}$	(Input, active low), $\overline{RESET}$ initializes the μPD7811.	
29	MODE0	Used as input in conjunction with MODE1 to select appropriate memory expansion mode. Also used to output $\overline{IO}$/M.	
30–31	X_2, X_1 (crystal)	This is a crystal connection terminal for system clock oscillation. When an external clock is supplied X_1 is the input.	
32	V_{SS}	Power supply ground potential.	
33	AV_{SS}	A/D converter power supply ground potential. Sets conversion's range lower limit.	

PIN IDENTIFICATION (cont.)

PIN NO.	PIN SYMBOL	FUNCTION
34–41	AN_0–AN_7	Eight analog inputs to the A/D converter. AN_7–AN_4 can also be used as a digital input port for falling edge detection.
42	V_{AREF}	Reference voltage for A/D converter. Sets conversion's range upper limit.
43	AV_{CC}	Power supply voltage for A/D converter.
44	$\overline{RD}$	(Three-state output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes high during Reset.
45	$\overline{WR}$	(Three-state output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes high during Reset.
46	ALE	The strobe signal is for latching the address signal to the output from PD_7–PD_0 when accessing external expansion memory.
47–54	PF_0–PF_7	Port F: (Three-state input/output) 8-bit programmable I/O port. Each line configurable independently as an input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
55–62	DB_0–DB_7	Port D: 8-bit programmable I/O port. This byte can be designated as either input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
63	$\overline{STOP}$	Input pin for hardware stop mode
64	V_{DD}	+5V power supply.

Notes: 1 clock cycle = 1 CL = 3/f.
1 machine cycle = 3 or 4 clock cycles.
1 instruction cycle = 1 to 19 machine cycles.
f: System clock frequency (MHz).

NEW INSTRUCTIONS

In addition to the existing instruction set for μPD7801, the following new instructions are incorporated in the μPD78C10/C11/C14:

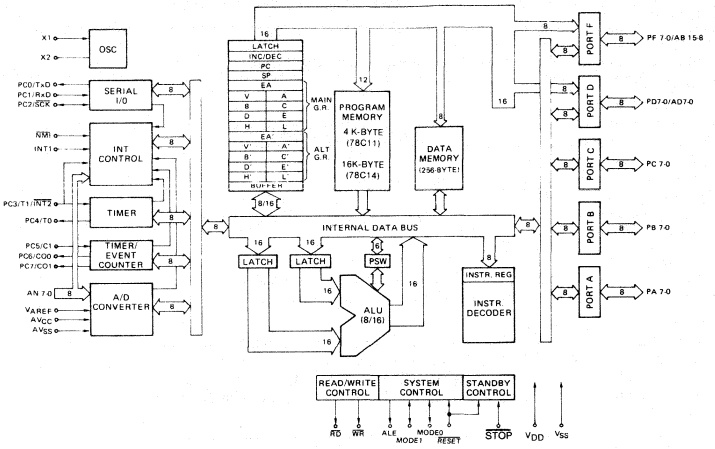
16-bit data transfer between memory and extended accumulator
16-bit data arithmetic and logical operation.

16-bit data addition and subtraction and 16-bit comparsion.
16-bit data shift and rotation
direct multiply and divide instructions.

8-bit by 8-bit division less then 8 μsec execution time.

16-bit divided by 8-bit less than 15 μsec execution
table look-up operation.
Register pair HL and DE are used as base register. Accumulator, B-register and extended accumulator are used as index register.
In addition to the 7811 instruction set, a STOP instruction is available.

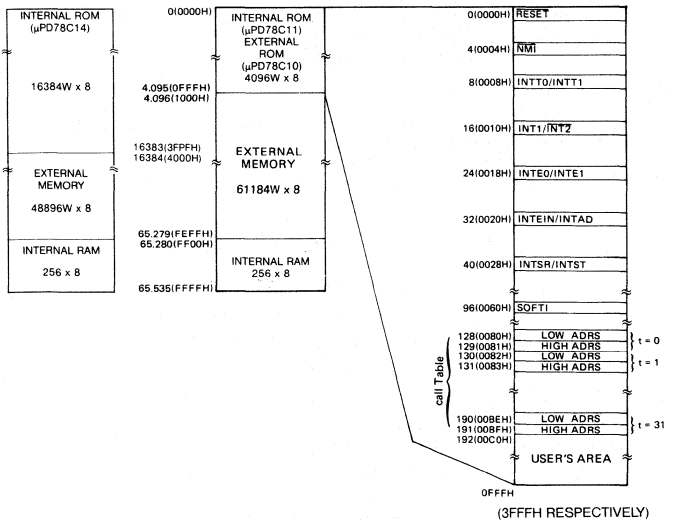
BLOCK DIAGRAM



Note: the μPD78C10 has no programmable ROM

MEMORY MAP

The μPD78C11 can directly address up to 64K-bytes of memory. Except for the on-chip ROM (0-4095) and RAM (65280–65535), any memory location can be used as ROM or RAM. The following memory map defines the 0-64K-byte memory space for the μPD78C11.



FUNCTIONAL DESCRIPTION

INPUT/OUTPUT

8 Analog Input Lines
44 Digital I/O Lines: five 8-bit ports (Port A, Port B, Port C, Port D, Port F) and 4 input lines (AN_4–AN_7)

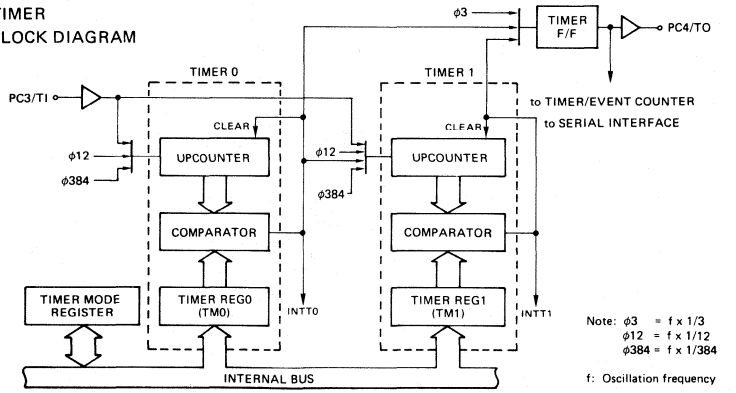
1. Analog Input Lines
   AN_0–AN_7 are configured as analog input lines for on-chip A/D converter.
2. Port Operation
   - Port A, Port B, Port C, Port F
     Each line of these ports can be individually programmed as an input or as an output. When used as I/O ports, all have latches outputs, high-impedance inputs.
   - Port D
     Port D can be programmed as a byte input or a byte output.
   - AN_4–AN_7
     The high-order analog input lines, AN_4–AN_7 can be used as digital input lines for falling edge detection.
3. Control Lines
   Under software control, each line of Port C can be configured individually to provide control lines for serial interface, timer and timer/counter, and interrupts.
4. Memory Expansion
   In addition to the single-chip operation mode the μPD78C11 has 4 memory expansion modes. Under software control, Port D can provide multiplexed low-order address and data bus and Port F can provide high-order address bus. The relation between memory expansion modes and the pin configurations of Port D and Port F is shown in the table that follows.

MEMORY EXPANSION		PORT CONFIGURATION
None	Port D Port F	I/O Port I/O Port
256 Bytes	Port D Port F	Multiplexed Address/Data Bus I/O Port
4K Bytes	Port D Port F_0–F_3 Port F_4–F_7	Multiplexed Address/Data Bus Address Bus I/O Port
16K Bytes	Port D Port F_0–F_5 Port F_6–F_7	Multiplexed/Data Bus Address Bus I/O Port
60K Bytes	Port D Port F	Multiplexed Address/Data Bus Address Bus

TIMERS

The timer/event counter consists of two 8-bit timers. The timers may be programmed independently or may be cascaded and used as a 16-bit timer. The timer can be set by software to increment at intervals of 4 machine cycles (1μs at 12MHz operation) or 128 machine cycles (32μs at 12MHz), or to increment on receipt of a pulse at TI.

TIMER
BLOCK DIAGRAM



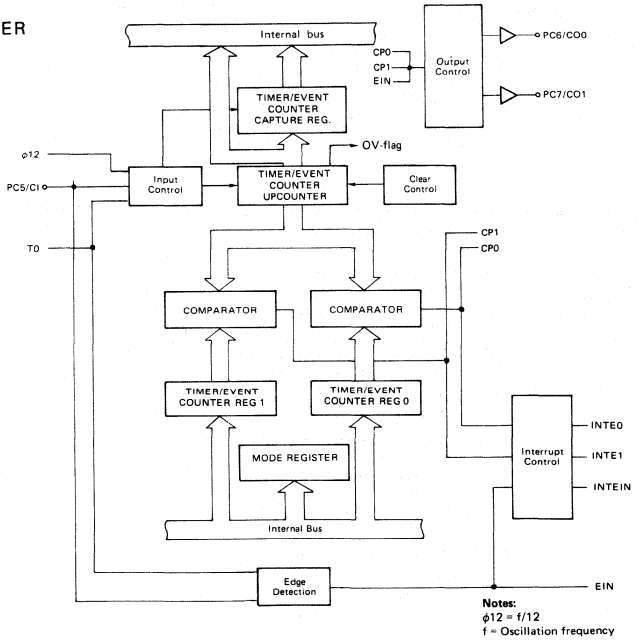
FUNCTIONAL DESCRIPTION (CONT.)

TIMER/EVENT COUNTER

The 16-bit Multifunctional timer/event counter can be used for the following operations:

- Interval timer
- External event counter
- Frequency measurement
- Pulse width measurement
- Programmable square-wave output
- Single pulse generation

TIMER/EVENT COUNTER BLOCK DIAGRAM

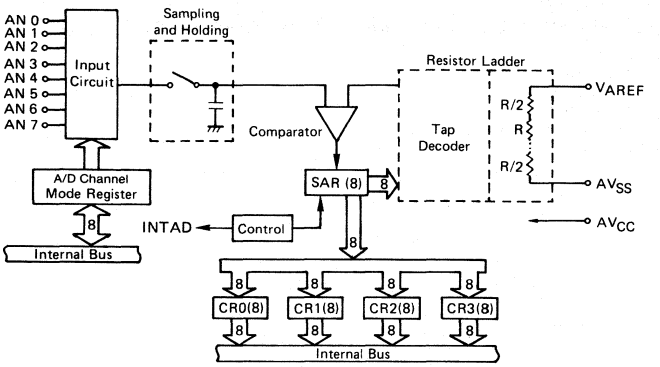


ANALOG/DIGITAL CONVERTER

- 8 Input Channels
- 4 Conversion Result Registers
- 2 Powerful Operation Modes
  - Auto Scan Mode
  - Channel Select Mode
- Successive Approximation Technique
- Absolute Accuracy ± 1.5 LSB (± 0.6%)
- Conversion Range 0 ~ 5V
- Conversion Time 50 μs
- Interrupt Generation

The μPD78C10/C11 features an 8-bit, high speed, high accuracy A/D converter. The A/D converter comprises a 256-Resistor Ladder and Successive Approximation Register (SAR). There are four conversion result registers (CR_0–CR_3). The 8-channel analog input may be operated in either of two modes. In the select mode, the conversion value of one analog input is sequentially stored in CR_0–CR_3. In the scan mode, the upper four channels or the lower four channels may be specified. Then those four channels will be consecutively selected and the conversion results stored sequentially in the four conversion result registers.

A/D CONVERTER BLOCK DIAGRAM

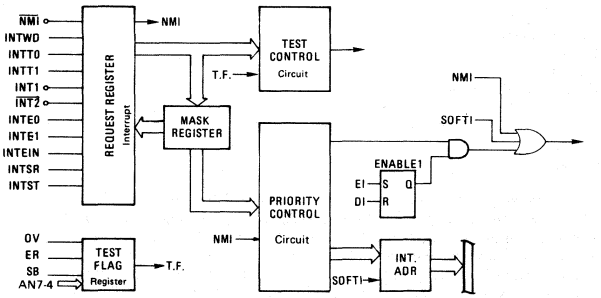


INTERRUPT STRUCTURE

There are 11 interrupt sources. Three are external interrupts and 8 are internal. These 11 interrupt sources are divided into 6 priority levels as shown in the table below.

INTERRUPT REQUEST	INTERRUPT VECTOR	TYPE OF INTERRUPT		IN/EXT
IRQ0	4	NMI	(Non-maskable interrupt)	External
IRQ1	8	INTT0 INTT1	(Coincidence signal from timer 0) (Coincidence signal from timer 1)	Internal
IRQ2	16	INT1 INT2	(Maskable intrrupt) (Maskable interrupr)	External
IRQ3	24	INTE0 INTE1	(Coincidence signal from timer/ event counter) Coincidence signal from timer/ event counter)	Internal
IRQ4	32	INTEIN INTAD	(Falling signal of C1 and T0 counter) (A/D converter interrupt)	In/External
IRQ5	40	INTSR INST	(Serial receive interrupt) (Serial send interrupt)	Internal

INTERRUPT CONTROL BLOCK DIAGRAM



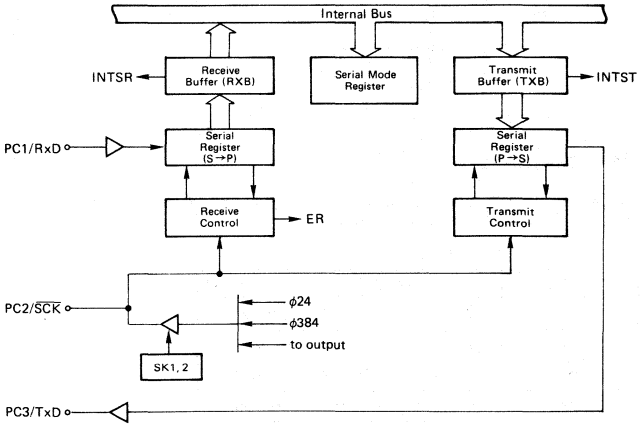
STANDBY FUNCTION

The μPD78C10/C11 offers a standby function that allows the user to save up to 32 bytes of RAM with backup power (V_{DD}) if the main power (V_{CC}) fails. On power up the μPD78C11 checks whether recovery was made from standby mode or from cold start.

UNIVERSAL SERIAL INTERFACE

The serial interface can operate in any of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first for ease of communication with certain peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception. In the search mode, data are transferred one bit at a time from serial register to receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from serial register to transmit buffer occurs 8 bits at a time.

UNIVERSAL SERIAL INTERFACE BLOCK DIAGRAM



Note: $\phi 24 = \frac{1}{24}$ f: oscillation frequency (MHz)

$\phi 384 = \frac{1}{384}$

ZERO-CROSSING DETECTOR

The INT1 and $\overline{INT2}$ terminals (used also as TI and PC_3) can be used to detect the zero-crossing point of slow moving AC signals. When driven directly, these pins respond as a normal digital input.

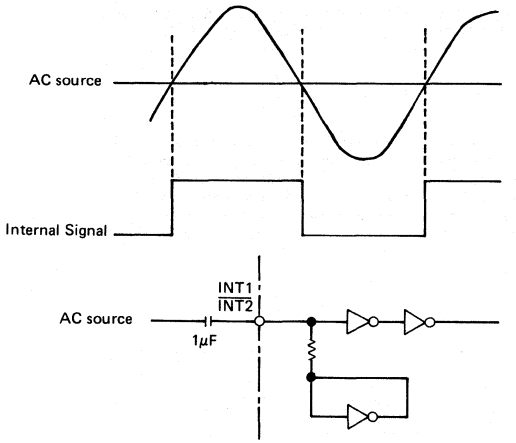
To utilize the zero-cross detection mode, an AC signal of approximately 1 – 1.8V peak-to-peak magnitude and a maximum frequency of 1kHz is coupled through an external capacitor to these pins.

For the INT1 pin, the internal digital state is sensed as a zero until the rising edge crosses the DC average level, when it becomes a one and INT1 interrupt is generated.

For the $\overline{INT2}$ pin, the state is sensed as a one until the falling edge crosses the DC average level, when it becomes a zero and $\overline{INT2}$ interrupt is generated.

The zero-cross detection capability allows the user to make the 50–60Hz power signal the basis for system timing and to control voltage phase sensitive devices.

In addition to the 7810/11 a register is implemented (ZCM = Zero Cross Mode Register) to allow to switch of the internal zero-cross detection circuit to reduce power consumption, especially during standby.



ZERO-CROSSING
DETECTION CIRCUIT

MODE0/MODE1-TERMINALS

The logic level applied to M0/M1-Terminals determines the memory map of μPD78C10/C11/C14 and the use of Port D/F as multiplexed Address/Data Bus.

M0	M1	MEMORY	ADDRESSES	LOCATION
0	1	4K	0 . . . . . FFFH	internal*
0	0	4K	0 . . . . . FFFH	external
0	1	16K	0 . . . . . 3FFFH	external
1	0	64K	0 . . . . . FEFFH	external

* MO, M1 = 0,1 realizes the ROM version (access of internal ROM), all others represent access of external memory only. In case external memory is used in addition to internal, memory mapping register has to be programmed then (see below).

MEMORY EXPANDES MODES	MEMORY MAPPING REGISTER MM2	MM1	MM0	NUMBER OF I/O LINES
Port Mode	0	0	X	44
256 Expanded	0	1	0	36
4K Expanded	1	0	0	32
16K Expanded	1	1	0	30
48K/60K Expanded	1	1	1	28

(using μPD7811)

Difference Between μPD78C11 and μPD7811

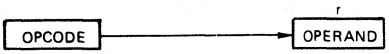
Item \ Product		μPD78C11	μPD7811
No. of instructions		159 (STOP instruction was added.)	158
No. of special registers		28 (ZCM register was added.)	27
Standby function		HALT MODE, software STOP mode, hardware STOP mode. In addition, in the software/hardware STOP mode, the internal RAM data (256 bytes) are retained at the power supply voltage as low as 2.5V	32 bytes of the 256-byte internal RAM data are retained at power supply voltage as low as 3.2V.
Control of zerocross detection circuit's selfbias		Available by setting the ZCM register	Not available
No. of states of the HLT instruction		12	11
Device construction		CMOS	NMOS
Power consumption	Operating	75mW TYP.	750mW TYP.
	Standby	5μW TYP.	4.8mW TYP.
Pin configuration		V_{DD} : Pin 64 $\overline{STOP}$: Pin 63	V_{CC}: Pin 64 V_{DD}: Pin 63

ADDRESSING MODES AND INSTRUCTION SET
μCOM 87AD
(μPD7810/7811/78PG11/7810H/7811H/ 78C10/78C11/78C14)

ADDRESS MODES

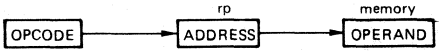
Register Addressing
Register Indirect Addressing
Auto-Increment Addressing
Auto-Decrement Addressing
Working Register Addressing
Direct Addressing
Immediate Addressing
Immediate Extended Addressing
Relative Addressing
Base Addressing
Base Index Addressing
Double Auto Increment Addressing

Register Addressing



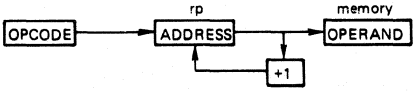
The instruction opcode specifies a register r which contains the operand.

Register Indirect Addressing



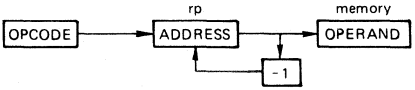
The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are using this address mode.

Auto-Increment Addressing

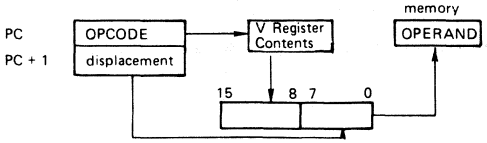


The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair is automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

Auto Decrement Addressing

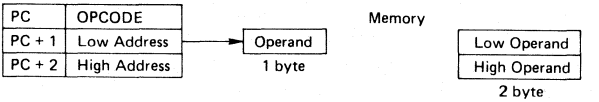


Working Register Addressing



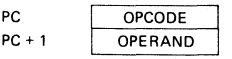
The contents of the register is linked with the byte following the opcode to form a memory address whose contents is the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only 1 additional byte is required for the address. Mnemonics with a W suffix are using this address mode.

Direct Addressing

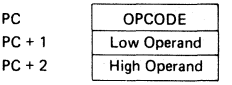


The two bytes following the opcode specify an address of a location containing the operand.

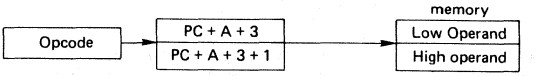
Immediate Addressing



Immediate Extended Addressing

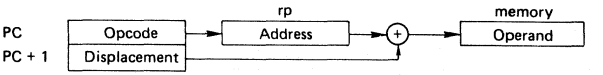


Relative Addressing



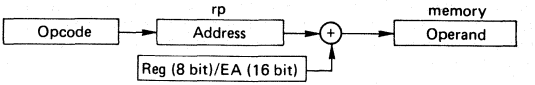
This addressing mode is used by the "Table"-command. It transfers the contents of 2 memory cells – addressed relatively to PC via the Accu A – into BC register-pair.
Application: Table look-up

Base-Addressing



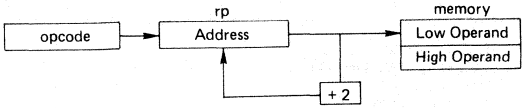
Register Pair DE or HL used as base pointer to the memory; immediate data (8 bit) or displacement added to the base.

Base-Index-Addressing



Register pair DE or HL used as base pointers to the memory; Register (8 bit) or Extended Accumulator (EA) as displacement added to the base.

Double auto increment



The opcode specifies the register pair which contains the memory address of the operand (16 bit). The contents of the register pair is automatically incremented by two to point to a new 16-bit operand.

μCOM 87 AD Instructionset

Operand Expression/Description

EXPRESSION	DESCRIPTION
r r1 r2	V, A, B, C, D, E, H, L EAH, EAL, B, C, D, E, H, L A, B, C
sr sr1 sr2 sr3 sr4	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, SML, EOM, ETMM, TMM, MM, MCC, MA, MB, MC, MF, TXB, TMO, TM1, ZCM (CMOS ONLY) PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM, RXB, CR0, CR1, CR2, CR3 PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM ETM0, ETM1 ECNT, ECPT
rp rp1 rp2 rp3	SP, B, D, H V, B, D, H, EA SP, B, D, H, EA B, D, H
rpa rpa1 rpa2 rpa3	B, D, H, D+, H+, D−, H− B, D, H B, D, H, D+, H+, D−, H−, D+byte, H+A, H+B, H+EA, H+byte D, H, D++, H++, D+byte, H+A, H+B, H+EA, H+byte
wa	8 bit immediate data
word byte bit	16 bit immediate data 8 bit immediate data 3 bit immediate data
f	CY, HC, Z
if	FNMI, FTO, FT1, F1, F2, FEO, FE1, FEIN, FAD, FSR, FST ER, OV, AN4, AN5, AN6, AN7, SB

Note 1

1. sr ~ sr4 (special register)

PA	:	PORT A	ECNT	:	TIMER/EVENT COUNTER UPCOUNTER
PB	:	PORT B			
PC	:	PORT C	ECPT	:	TIMER/EVENT COUNTER CAPTURE
PD	:	PORT D			
PF	:	PORT F	ETMM	:	TIMER/EVENT COUNTER MODE
MA	:	MODE A			
MB	:	MODE B	EOM	:	TIMER/EVENT COUNTER OUTPUT MODE
MC	:	MODE C			
MCC	:	MODE CONTROL C	ANM	:	A/D CHANNEL MODE
MF	:	MODE F	CRO	:	A/D CONVERSION RESULTO ~ 3
MM	:	MEMORY MAPPING	~		
TMO	:	TIMER REGO	CR3		
TM1	:	TIMER REG1	TXB	:	Tx BUFFER
TMM	:	TIMER MODE	RXB	:	Rx BUFFER
ETMO	:	TIMER/EVENT COUNTER REGO	SMH	:	SERIAL MODE High
			SML	:	SERIAL MODE Low
ETM1	:	TIMER/EVENT COUNTER REG1	MKH	:	MASK High
			MKL	:	MASK Low
ZCM	:	ZERO CROSS MODE (CMOS ONLY)			

2. rp ~ rp3 (register pair)

SP	:	STACK POINTER
B	:	BC
D	:	DE
H	:	HL
V	:	VA
EA	:	EXTENDED ACCUMULATOR

3. rpa ~ rpa3 (rp addressing)

B	:	(BC)
D	:	(DE)
H	:	(HL)
D+	:	$(DE)^{+}$
H+	:	$(HL)^{+}$
D−	:	$(DE)^{-}$
H−	:	$(HL)^{-}$
D++	:	$(DE)^{++}$
H++	:	$(HL)^{++}$
D+byte	:	(DE+byte)
H+A	:	(HL+A)
H+B	:	(HL+B)
H+EA	:	(HL+EA)
H+byte	:	(HL+byte)

4. f (flag)

CY	:	CARRY
HC	:	HALF CARRY
Z	:	ZERO

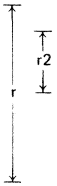
5. if (Interrupt flag)

FNMI	:	INTFNMI
FT0	:	INTFT0
FT1	:	INTFT1
F1	:	INTF1
F2	:	INTF2
FE0	:	INTFE0
FE1	:	INTFE1
FEIN	:	INTFEIN
FAD	:	INTFAD
FSR	:	INTFSR
FST	:	INTFST
ER	:	ERROR
OV	:	OVERFLOW
AN4	:	ANALOG INPUT 4~7
~		
AN7	:	
SB	:	STANDBY

Description of Instruction Code Symbols

r

R_2	R_1	R_0	reg
0	0	0	V
0	0	1	A
0	1	0	B
0	1	1	C
1	0	0	D
1	0	1	E
1	1	0	H
1	1	1	L

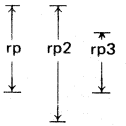


r1

T_2	T_1	T_0	reg
0	0	0	EAH
0	0	1	EAL
0	1	0	B
0	1	1	C
1	0	0	D
1	0	1	E
1	1	0	H
1	1	1	L

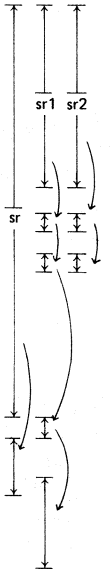
rp

P_2	P_1	P_0	reg-pair
0	0	0	SP
0	0	1	BC
0	1	0	DE
0	1	1	HL
1	0	0	EA



sr

S_5	S_4	S_3	S_2	S_1	S_0	Special-reg
0	0	0	0	0	0	PA
0	0	0	0	0	1	PB
0	0	0	0	1	0	PC
0	0	0	0	1	1	PD
0	0	0	1	0	1	PF
0	0	0	1	1	0	MKH
0	0	0	1	1	1	MKL
0	0	1	0	0	0	ANM
0	0	1	0	0	1	SMH
0	0	1	0	1	0	SML
0	0	1	0	1	1	EOM
0	0	1	1	0	0	ETMM
0	0	1	1	0	1	TMM
0	1	0	0	0	0	MM
0	1	0	0	0	1	MCC
0	1	0	0	1	0	MA
0	1	0	0	1	1	MB
0	1	0	1	0	0	MC
0	1	0	1	1	1	MF
0	1	1	0	0	0	TXB
0	1	1	0	0	1	RXB
0	1	1	0	1	0	TM0
0	1	1	0	1	1	TM1
1	0	1	0	0	0	ZCM (CMOS)
1	0	0	0	0	0	CR0
1	0	0	0	0	1	CR1
1	0	0	0	1	0	CR2
1	0	0	0	1	1	CR3

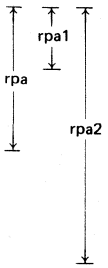


rp1

Q_2	Q_1	Q_0	reg-pair
0	0	0	VA
0	0	1	BC
0	1	0	DE
0	1	1	HL
1	0	0	EA

rpa

A_3	A_2	A_1	A_0	addressing
0	0	0	0	–
0	0	0	1	(BC)
0	0	1	0	(DE)
0	0	1	1	(HL)
0	1	0	0	$(DC)^+$
0	1	0	1	$(HL)^+$
0	1	1	0	$(DC)^-$
0	1	1	1	$(HL)^-$
1	0	1	1	(DE+byte)
1	1	0	0	(HL+A)
1	1	0	1	(HL+B)
1	1	1	0	(HL+EA)
1	1	1	1	(HL+byte)



rpa3

C_3	C_2	C_1	C_0	addressing
0	0	0	0	(DE)
0	0	0	1	(HL)
0	0	1	0	$(DE)^{++}$
0	0	1	1	$(HL)^{++}$
1	0	1	1	(DE+byte)
1	1	0	0	(HL+A)
1	1	0	1	(HL+B)
1	1	1	0	(HL+EA)
1	1	1	1	(HL+byte)

sr3

U_0	Special-reg
0	ETM0
1	ETM1

sr4

V_0	Special-reg
0	ECNT
1	ECPT

List of Mode Registers

MODE REGISTER	READ/WRITE	FUNCTION
MA register (Mode A)	W	An 8 bit register for designating the input/output of the port A in units of bit.
MB register (Mode B)	W	An 8 bit register for designating the input/output of the port B in units of bit.
MCC register (Mode Control C)	W	An 8 bit register for designating the port/control mode of the port C in units of bit.
MC register (Mode C)	W	An 8 bit register for designating the input/output of the port C in units of bit.
MM register (Memory Mapping)	W	A 4 bit register for designating the port/expansion mode od port D and port F.
MF register (Mode F)	W	An 8 bit register for designating the input of port F in units of bit.
TMM register (Timer Mode Reg.)	R/W	An 8 bit register for designating the operation mode of timer.
ETMM register (Timer/Event Counter Mode Reg.)	W	An 8 bit for designating the operation mode of timer/event counter.
EOM register (Timer/Event Counter Output Mode Reg.)	R/W	An 8 bit register for controlling the ouput level of CO0, CO1.
SMH register	R/W	7 bit and 8 bit registers for designating the operation mode of serial interface.
SML	W	
ANM register (A/D Channel Mode Reg.)	R/W	An 5 bit register for designating the operation mode of A/D converter and for indicating the input channel during A/D conversion.
ZCM register (Zero Cross Mode Reg.) CMOS only	W	A 2 bit register for switching on/off the internal zero cross detection circuit.

f

F_2	F_1	F_0	INTF
0	0	0	–
0	1	0	CY
0	1	1	HC
1	0	0	Z

if

I_4	I_3	I_2	I_1	I_0	INTF
0	0	0	0	0	INTENMI
0	0	0	0	1	INTFT0
0	0	0	1	0	INTFT1
0	0	0	1	1	INTF1
0	0	1	0	0	INTF2
0	0	1	0	1	INTFE0
0	0	1	1	0	INTFE1
0	0	1	1	1	INTFEIN
0	1	0	0	0	INTFAD
0	1	0	0	1	INTFSR
0	1	0	1	0	INTFST
0	1	0	1	1	ER
0	1	1	0	0	OV
1	0	0	0	0	AN4
1	0	0	0	1	AN5
1	0	0	1	0	AN6
1	0	0	1	1	AN7
1	0	1	0	0	SB

INSTRUCTION SET

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
8-BIT DATA TRANSFER			r1, A	0 0 0 1 1 T_2 T_1 T_0				4	r1 ← A	
			A, r1	0 0 0 0 1 T_2 T_1 T_0				4	A ← r1	
		*	sr, A	0 1 0 0 1 1 0 1	1 1 S_5 S_4 S_3 S_2 S_1 S_0			10	sr ← A	
		*	A, sr1	0 1 0 0 1 1 0 0	1 1 S_5 S_4 S_3 S_2 S_1 S_0			10	A ← sr1	
	MOV		r, word	0 1 1 1 0 0 0 0	0 1 1 0 1 R_2 R_1 R_0	Low Adrs	High Adrs	17	r ← (word)	
			word, r	0 1 1 1 0 0 0 0	0 1 1 1 1 R_2 R_1 R_0	Low Adrs	High Adrs	17	(word) ← r	
		*	r, byte	0 1 1 0 1 R_2 R_1 R_0	Data			7	r ← byte	
	MVI		sr2, byte	0 1 1 0 0 1 0 0	S_3 0 0 0 0 S_2 S_1 S_0	Data		14	sr2 ← byte	
	MVIW	*	wa, byte	0 1 1 1 0 0 0 1	Offset	Data		13	(V,wa) ← byte	
	MVIX	*	rpa1, byte	0 1 0 0 1 0 A_1 A_0	Data			10	(rpa1) ← byte	
	STAW	*	wa	0 1 1 0 0 0 1 1	Offset			10	(V.wa) ← A	
	LDAW	*	wa	0 0 0 0 0 0 0 1	Offset			10	A ← (V.wa)	
	STAX	*	rpa2	A_3 0 1 1 1 A_2 A_1 A_0	Data (*1)			7/13	(rpa2) ← A	
	LDAX	*	rpa2	A_3 0 1 0 1 A_2 A_1 A_0	Data (*1)			7/13	A ← (rpa2)	
	EXX			0 0 0 1 0 0 0 1				4	B ↔ B', C ↔ C', D ↔ D', E ↔ E', H ↔ H', L ↔ L'	
	EXA			0 0 0 1 0 0 0 0				4	V, A ↔ V', A', EA ↔ EA'	
	EXH			0 1 0 1 0 0 0 0				4	H, L ↔ H', L'	

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
16-BIT DATA TRANSFER	BLOCK		D+	0 0 1 1 0 0 0 1				13 x (C+1)	(DE)+ ← (HL)+, C ← C−1 End if borrow	
	DMOV		rp3, EA	1 0 1 1 0 1 P_1 P_0				4	$rp3_L$ ← EAL, $rp3_H$ ← EAH	
			EA, rp3	1 0 1 0 0 1 P_1 P_0				4	EAL ← $rp3_L$, EAH ← $rp3_H$	
			sr3, EA	0 1 0 0 1 0 0 0	1 1 0 1 0 0 1 U_0			14	sr3 ← EA	
			EA, sr4	↓ ↓	1 1 0 0 0 0 0 V_0			14	EA ← sr4	
	SBCD		word	0 1 1 1 0 0 0 0	0 0 0 1 1 1 1 0	Low Adrs	High Adrs	20	(word) ← C, (word+1) ← B	
	SDED		word		0 0 1 0 1 1 1 0			20	(word) ← E, (word+1) ← D	
	SHLD		word		0 0 1 1 1 1 1 0			20	(word) ← L, (word+1) ← H	
	SSPD		word		0 0 0 0 1 1 1 0	↓	↓	20	(word) ← SP_L, (word+1) ← SP_H	
	STEAX		rpa3	0 1 0 0 1 0 0 0	1 0 0 1 C_3 C_2 C_1 C_0	Data (*2)		14/20	(rpa3) ← EAL, (rpa3+1) ← EAH	
	LBCD		word	0 1 1 1 0 0 0 0	0 0 0 1 1 1 1 1	Low Adrs	High Adrs	20	C ← (word), B ← (word+1)	
	LDED		word		0 0 1 0 1 1 1 1			20	E ← (word), D ← (word+1)	
	LHLD		word		0 0 1 1 1 1 1 1			20	L ← (word), H ← (word+1)	
	LSPD		word		0 0 0 0 1 1 1 1	↓	↓	20	SP_L ← (word), SP_H ← (word+1)	
	LDEAX		rpa3	0 1 0 0 1 0 0 0	1 0 0 0 C_3 C_2 C_1 C_0	Data (*2)		14/20	EAL ← (rpa3), EAH ← (rpa3+1)	
	PUSH		rp1	1 0 1 1 0 Q_2 Q_1 Q_0				13	(SP−1) ← $rp1_H$, (SP−2) ← $rp1_L$ SP ← SP−2	
	POP		rp1	1 0 1 0 0 Q_2 Q_1 Q_0				10	$rp1_L$ ← (SP), $rp1_H$ ← (SP+1) SP ← SP+2	
	LXI	*	rp2, word	0 P_2 P_1 P_0 0 1 0 0	Low Byte	High Byte		10	rp2 ← word	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
	TABLE		01001000	10101000			17	C ← (PC+3+A) B ← (PC+3+A+1)	
8-BIT ARITHMETIC (REGISTER)	ADD	A, r	01100000	11000 R_2 R_1 R_0			8	A ← A+r	
		r, A		01000 R_2 R_1 R_0			8	r ← r+A	
	ADC	A, r		11010 R_2 R_1 R_0			8	A ← A+r+CY	
		r, A		01010 R_2 R_1 R_0			8	r ← r+A+CY	
	ADDNC	A, r		10100 R_2 R_1 R_0			8	A ← A+r	No Carry
		r, A		00100 R_2 R_1 R_0			8	r ← r+A	No Carry
	SUB	A, r		11100 R_2 R_1 R_0			8	A ← A−r	
		r, A		01100 R_2 R_1 R_0			8	r ← r−A	
	SBB	A, r		11110 R_2 R_1 R_0			8	A ← A−r−CY	
		r, A		01110 R_2 R_1 R_0			8	r ← r−A−CY	
	SUBNB	A, r		10110 R_2 R_1 R_0			8	A ← A−r	No Borrow
		r, A		00110 R_2 R_1 R_0			8	r ← r−A	No Borrow
	ANA	A, r		10001 R_2 R_1 R_0			8	A ← A ∧ r	
		r, A		00001 R_2 R_1 R_0			8	r ← r ∧ A	
	ORA	A, r		10011 R_2 R_1 R_0			8	A ← A ∨ r	
		r, A		00011 R_2 R_1 R_0			8	r ← r ∨ A	
	XRA	A, r		10010 R_2 R_1 R_0			8	A ← A ∨̄ r	
		r, A		00010 R_2 R_1 R_0			8	r ← r ∨̄ A	
	GTA	A, r		10101 R_2 R_1 R_0			8	A−r−1	No Borrow
		r, A	↓ ↓	00101 R_2 R_1 R_0			8	r−A−1	No Borrow

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
8-BIT ARITHMETIC (REG.)	LTA	A, r	01100000	10111 R_2 R_1 R_0			8	A−r	Borrow
		r, A		00111 R_2 R_1 R_0			8	r−A	Borrow
	NEA	A, r		11101 R_2 R_1 R_0			8	A−r	No Zero
		r, A		01101 R_2 R_1 R_0			8	r−A	No Zero
	EQA	A, r		11111 R_2 R_1 R_0			8	A−r	Zero
		r, A		01111 R_2 R_1 R_0			8	r−A	Zero
	ONA	A, r		11001 R_2 R_1 R_0			8	A ∧ r	No Zero
	OFFA	A, r	↓ ↓	11011 R_2 R_1 R_0			8	A ∧ r	Zero
8-BIT ARITHMETIC (MEMORY)	ADDX	rpa	01110000	11000 A_2 A_1 A_0			11	A ← A+ (rpa)	
	ADCX	rpa		11010 A_2 A_1 A_0			11	A ← A+ (rpa)+CY	
	ADDNCX	rpa		10100 A_2 A_1 A_0			11	A ← A+ (rpa)	No Carry
	SUBX	rpa		11100 A_2 A_1 A_0			11	A ← A− (rpa)	
	SBBX	rpa		11110 A_2 A_1 A_0			11	A ← A− (rpa)−CY	
	SUBNBX	rpa		10110 A_2 A_1 A_0			11	A ← A− (rpa)	No Borrow
	ANAX	rpa		10001 A_2 A_1 A_0			11	A ← A ∧ (rpa)	
	ORAX	rpa		10011 A_2 A_1 A_0			11	A ← A ∨ (rpa)	
	XRAX	rpa		10010 A_2 A_1 A_0			11	A ← A ∨̄ (rpa)	
	GTAX	rpa		10101 A_2 A_1 A_0			11	A− (rpa)−1	No Borrow
	LTAX	rpa	↓ ↓	10111 A_2 A_1 A_0			11	A− (rpa)	Borrow

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	NEI	*	A, byte	01100111	← Data →			7	A–byte	No Zero
			r, byte	01110100	01101 R_2 R_1 R_0	Data		11	r–byte	No Zero
			sr2, byte	0110 ↓	S_3 1101 S_2 S_1 S_0	↓		14	sr2–byte	No Zero
	EQI	*	A, byte	01110111	← Data →			7	A–byte	Zero
			r, byte	01110100	01111 R_2 R_1 R_0	Data		11	r–byte	Zero
			sr2, byte	0110 ↓	S_3 1111 S_2 S_1 S_0	↓		14	sr2–byte	Zero
	ONI	*	A, byte	01000111	← Data →			7	A ∧ byte	No Zero
			r, byte	01110100	01001 R_2 R_1 R_0	Data		11	r ∧ byte	No Zero
			sr2, byte	0110 ↓	S_3 1001 S_2 S_1 S_0	↓		14	sr2 ∧ byte	No Zero
	OFFI	*	A, byte	01010111	← Data →			7	A ∧ byte	Zero
			r, byte	01110100	01011 R_2 R_1 R_0	Data		11	r ∧ byte	Zero
			sr2, byte	0110 ↓	S_3 1011 S_2 S_1 S_0	↓		14	sr2 ∧ byte	Zero
WORKING REGISTER	ADDW		wa	01110100	11000000	Offset		14	A ← A+(V.wa)	
	ADCW		wa	↓	1101	↓		14	A ← A+(V.wa)+CY	
	ADDNCW		wa	↓	1010	↓		14	A ← A+(V.wa)	No Carry
	SUBW		wa	↓	1110	↓		14	A ← A–(V.wa)	
	SBBW		wa	↓	1111	↓		14	A ← A–(V.wa)–CY	
	SUBNBW		wa	↓	1011 ↓	↓		14	A ← A–(V.wa)	No Borrow
	ANAW		wa	↓	10001000	↓		14	A ← A ∧ (V.wa)	
	ORAW		wa	↓	1001 ↓	↓		14	A ← A ∨ (V.wa)	

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
WORKING REGISTER	XRAM		wa	01110100	10010000	Offset		14	A ← A ∀ (V.wa)	
	GTAW		wa	↓	10101000	↓		14	A–(V.wa)–1	No Borrow
	LTAW		wa	↓	1011	↓		14	A–(V.wa)	Borrow
	NEAW		wa	↓	1110	↓		14	A–(V.wa)	No Zero
	EQAW		wa	↓	1111	↓		14	A–(V.wa)	Zero
	ONAW		wa	↓	1100	↓		14	A ∧ (V.wa)	No Zero
	OFFAW		wa	↓ ↓	1101 ↓	↓		14	A ∧ (V.wa)	Zero
	ANIW	*	wa, byte	00000101	← Offset →	Data		19	(V.wa) ← (V.wa) ∧ byte	
	ORIW	*	wa, byte	0001	↓	↓		19	(V.wa) ← (V.wa) ∨ byte	
	GTIW	*	wa, byte	0010	↓	↓		13	(V.wa)–byte–1	No Borrow
	LTIW	*	wa, byte	0011	↓	↓		13	(V.wa)–byte	Borrow
	NEIW	*	wa, byte	0110	↓	↓		13	(V.wa)–byte	No Zero
	EQIW	*	wa, byte	0111	↓	↓		13	(V.wa)–byte	Zero
	ONIW	*	wa, byte	0100	↓	↓		13	(V.wa) ∧ byte	No Zero
	OFFIW	*	wa, byte	0101 ↓	↓	↓		13	(V.wa) ∧ byte	Zero
16-BIT ARITHMETIC	EADD		EA, r2	01110000	010000 R_1 R_0			11	EA ← EA+r2	
	DADD		EA, rp3	0100	110001 P_1 P_0			11	EA ← EA+rp3	
	DADC		EA, rp3	↓	1101			11	EA ← EA+rp3+CY	
	DADDNC		EA, rp3	↓	1010 ↓			11	EA ← EA+rp3	No Carry
	ESUB		EA, r2	↓ 0000	011000 R_1 R_0			11	EA ← EA–r2	

	MNEMONIC	OPERAND	OP CODE B1	B2	B3	B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	NEAX	rpa	01110000	11101 A_2 A_1 A_0			11	A– (rpa)	No Zero
	EQAX	rpa		11111 A_2 A_1 A_0			11	A– (rpa)	Zero
	ONAX	rpa		11001 A_2 A_1 A_0			11	A ∧ (rpa)	No Zero
	OFFAX	rpa	↓ ↓	11011 A_2 A_1 A_0			11	A ∧ (rpa)	Zero
	ADI *	A, byte	01000110	← Data →			7	A ← A+byte	
		r, byte	01110100	01000 R_2 R_1 R_0	Data		11	r ← r+byte	
		sr2, byte	0110 ↓	S_3 1000 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte	
	ACI *	A, byte	01010110	← Data →			7	A ← A+byte+CY	
		r, byte	01110100	01010 R_2 R_1 R_0	Data		11	r ← r+byte+CY	
		sr2, byte	0110 ↓	S_3 1010 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte+CY	
	ADINC *	A, byte	00100110	← Data →			7	A ← A+byte	No Carry
		r, byte	01110100	00100 R_2 R_1 R_0	Data		11	r ← r+byte	No Carry
		sr2, byte	0110 ↓	S_3 0100 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte	No Carry
	SUI *	A, byte	01100110	← Data →			7	A ← A–byte	
		r, byte	01110100	01100 R_2 R_1 R_0	Data		11	r ← r–byte	
		sr2, byte	0110 ↓	S_3 1100 S_2 S_1 S_0	↓		20	sr2 ← sr2–byte	
	SBI *	A, byte	01110110	← Data →			7	A ← A–byte–CY	
		r, byte	01110100	01110 R_2 R_1 R_0	Data		11	r ← r–byte–CY	
		sr2, byte	0110 ↓	S_3 1110 S_2 S_1 S_0	↓		20	sr2 ← sr2–byte–CY	

	MNEMONIC	OPERAND	OP CODE B1	B2	B3	B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	SUINB *	A, byte	00110110	← Data →			7	A ← A–byte	No Borrow
		r, byte	01110100	00110 R_2 R_1 R_0	Data		11	r ← r–byte	No Borrow
		sr2, byte	0110 ↓	S_3 0110 S_2 S_1 S_0	↓		20	sr2 ← sr2–byte	No Borrow
	ANI *	A, byte	00000111	← Data →			7	A ← A ∧ byte	
		r, byte	01110100	00001 R_2 R_1 R_0	Data		11	r ← r ∧ byte	
		sr2, byte	01100100	S_3 0001 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∧ byte	
	ORI *	A, byte	00010111	← Data →			7	A ← A ∨ byte	
		r, byte	01110100	00011 R_2 R_1 R_0	Data		11	r ← r ∨ byte	
		sr2, byte	0110 ↓	S_3 0011 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∨ byte	
	XRI *	A, byte	00010110	← Data →			7	A ← A ∨̄ byte	
		r, byte	01110100	00010 R_2 R_1 R_0	Data		11	r ← r ∨̄ byte	
		sr2, byte	0110 ↓	S_3 0010 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∨̄ byte	
	GTI *	A, byte	00100111	← Data →			7	A–byte–1	No Borrow
		r, byte	01110100	00101 R_2 R_1 R_0	Data		11	r–byte–1	No Borrow
		sr2, byte	0110 ↓	S_3 0101 S_2 S_1 S_0	↓		14	sr2–byte–1	No Borrow
	LTI *	A, byte	00110111	← Data →			7	A–byte	Borrow
		r, byte	01110100	00111 R_2 R_1 R_0	Data		11	r–byte	Borrow
		sr2, byte	0110 ↓	S_3 0111 S_2 S_1 S_0	↓		14	sr2–byte	Borrow

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
16-BIT ARITHMETIC	DSUB	EA, rp3	01110100	111001 P_1 P_0			11	EA ← EA−rp3	
	DSBB	EA, rp3		1111			11	EA ← EA−rp3−CY	
	DSUBNB	EA, rp3		1011			11	EA ← EA−rp3	No Borrow
	DAN	EA, rp3		100011 P_1 P_0			11	EA ← EA ∧ rp3	
	DOR	EA, rp3		1001			11	EA ← EA ∨ rp3	
	DXR	EA, rp3		100101 P_1 P_0			11	EA ← EA ∨ rp3	
	DGT	EA, rp3		101011 P_1 P_0			11	EA−rp3−1	No Borrow
	DLT	EA, rp3		1011			11	EA−rp3	Borrow
	DNE	EA, rp3		1110			11	EA−rp3	No Zero
	DEQ	EA, rp3		1111			11	EA−rp3	Zero
	DON	EA, rp3		1100			11	EA ∧ rp3	No Zero
	DOFF	EA, rp3		1101			11	EA ∧ rp3	Zero
MULTIP./DIVIDE	MUL	r2	01001000	001011 R_1 R_0			32	EA ← A X r2	
	DIV	r2		0011			59	EA ← EA÷r2, r2 ← surplus	
INCREMENT/DECREMENT	INR	r2	010000 R_1 R_0				4	r2 ← r2+1	Carry
	INRW *	wa	00100000	← Offset →			16	(V.wa) ← (V.wa)+1	Carry
	INX	rp	00 P_1 P_0 0010				7	rp ← rp+1	
		EA	10101000				7	EA ← EA+1	
	DCR	r2	010100 R_1 R_0				4	r2 ← r2−1	Borrow
	DCRW *	wa	00110000	← Offset →			16	(V.wa) ← (V.wa)−1	Borrow

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
ROTATE AND SHIFT	DCX	rp	00 P_1 P_0 0011				7	rp ← rp−1	
		EA	10101001				7	EA ← EA−1	
	RLL	r2	01001000	001101 R_1 R_0			8	$r2_{m+1}$ ← $r2_m$, $r2_0$ ← CY, CY ← $r2_7$	
	RLR	r2		00 R_1 R_0			8	$r2_{m-1}$ ← $r2_m$, $r2_7$ ← CY, CY ← $r2_0$	
	SLL	r2		001001 R_1 R_0			8	$r2_{m+1}$ ← $r2_m$, $r2_0$ ← 0, CY ← $r2_7$	
	SLR	r2		00 R_1 R_0			8	$r2_{m-1}$ ← $r2_m$, $r2_7$ ← 0, CY ← $r2_0$	
	SLLC	r2		000001 R_1 R_0			8	$r2_{m+1}$ ← $r2_m$, $r2_0$ ← 0, CY ← $r2_7$	Carry
	SLRC	r2		00 R_1 R_0			8	$r2_{m-1}$ ← $r2_m$, $r2_7$ ← 0, CY ← $r2_0$	Carry
	DRLL	EA		10110100			8	EA_{n+1} ← EA_n, EA_0 ← CY, CY ← EA_{15}	
	DRLR	EA		0000			8	EA_{n-1} ← EA_n, EA_{15} ← CY, CY ← EA_0	
	DSLL	EA		10100100			8	EA_{n+1} ← EA_n, EA_0 ← 0, CY ← EA_{15}	
	DSLR	EA		0000			8	EA_{n-1} ← EA_n, EA_{15} ← 0, CY ← EA_0	
	DAA		01100001				4	Decimal Adjust Accumulator	
	STC		01001000	00101011			8	CY ← 1	
	CLC			00101010			8	CY ← 0	
	NEGA			00111010			8	A ← A+1	
	RLD		01001000	00111000			17	Rotate Left Digit	
	RRD			1001			17	Rotate Right Digit	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
JUMP	JMP *	word	01010100	← Low Adrs →	High Adrs		10	PC ← word	
	JB		00100001				4	PC_H ← B, PC_L ← C	
	JR	word	11 ← jdispl →				10	PC ← PC+1+jdispl	
	JRE *	word	0100111 ← jdisp →				10	PC ← PC+2+jdispl	
	JEA		01001000	00101000			8	PC ← EA	
CALL	CALL *	word	01000000	← Low adrs →	High Adrs		16	(SP−1) ← $(PC+3)_H$, (SP−2) ← $(PC+3)_L$ PC ← word, SP ← SP−2	
	CALB		01001000	00101001			17	(SP−1) ← $(PC+2)_H$, (SP−2) ← $(PC+2)_L$ PC_H ← B, SP ← SP−2, PC_L ← C	
	CALF *	word	01111 ← fa →				13	(SP−1) ← $(PC+2)_H$, (SP−2) ← $(PC+2)_L$ PC_{15-11} ← 00001, PC_{10-0} ← fa, SP ← SP−2	
	CALT	word	100 ← ta →				16	(SP−1) ← $(PC+1)_H$, (SP−2) ← $(PC+1)_L$ PC_L ← (128+2ta), PC_H ← (129+2ta), SP ← SP−2	
	SOFTI		01110010				16	(SP−1) ← PSW, (SP−2) ← $(PC+1)_H$, (SP−3) ← $(PC+1)_L$, PC ← 0060H, SP ← SP−3	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
RETURN	RET		10111000				10	PC_L ← (SP), PC_H ← (SP+1) SP ← SP+2	
	RETS		1001				10	PC_L ← (SP), PC_H ← (SP+1) SP ← SP+2, PC ← PC+n	
	RETI		01100013				13	PC_L ← (SP), PC_H ← (SP+1) PSW ← (SP+2), SP ← SP+3	Unconditional Skip
SKIP	SK	f	01001000	00001 F_2 F_1 F_0			8	Skip if f=1	f=1
	SKN	f		0001			8	Skip if f=0	f=0
	SKIT	irf		0101 I_4 I_3 I_2 I_1 I_0			8	Skip if irf=1, then reset irf	irf=1
	SKNIT	irf		0111 I_4 I_3 I_2 I_1 I_0			8	Skip if irf=0 Reset irf, if irf=1	irf=0
CPU CONTROL	NOP		00000000				4	No Operation	
	EI		10101010				4	Enable Interrupt	
	DI		10111010				4	Disable Interrupt	
	HLT		01001000	00111011			11	Halt	

Notes:

(*1): B2(Data) : rpa2 = D+byte, H+byte
(*2): B3(Data) : rpa3 = D+byte, H+byte
(*3): right side of slash (/) in states indicates case rpa2, rpa3 = D+byte, H+A, H+B, H+EA, H+byte
(*4): in the case of skip condition, the idle states are as follows.

1-byte instruction : 4 states — 2-byte instruction (with *) : 7 states
2-byte instruction : 8 states — 3-byte instruction (with *) : 10 states
3-byte instruction : 11 states — 4-byte instruction : 14 states

Additional instruction for μPD78C10/C11/C14:

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
	STOP		01001000	10111011			12	Stop	

NEC

ELECTRICAL SPECIFICATIONS
AND PACKAGE OUTLINES FOR
μPD7810/7811/78PG11E

ABSOLUTE MAXIMUM RATINGS

(T_a = 25° C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power Supply Voltage	V_{CC}		−0.5 to +7.0	V
	V_{DD}		−0.5 to +7.0	V
	AV_{CC}		−0.5 to +7.0	V
	AV_{SS}		−0.5 to +0.5	V
Input Voltage	V_I		−0.5 to +7.0	V
Output Voltage	V_O		−0.5 to + 7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−0.5	mA
		All Output Pin Total	−20	mA
Reference Input Voltage	V_{AREF}		−0.5 to V_{CC}	V
Operating Temperature	T_{opt}	10 MHz < f_{XTAL} ≤ 12 MHz	−10 to +70	°C
		f_{XTAL} ≤ 10 MHz	−40 to + 85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

OPERATING CONDITION

PARAMETER / OSC. FREQ.	T_a	V_{CC}, AV_{CC}
10 MHz < f_{XTAL} ≤ 12 MHz	−10°C to +70°C	+5.0V ± 5 %
f_{XTAL} ≤ 10 MHz	−40°C to +85°C	+5.0V ± 10 %

CAPACITANCE

(T_a = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_c = 1 MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	$C_{I/O}$				20	pF

DC CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1 and X2	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1, X2 *1	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ V_{IN} ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) 0V ≤ V_{IN} ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	0.45V ≤ V_O ≤ V_{CC}			± 10	μA
AV_{CC} Supply Current	AI_{CC}			6	12	mA
V_{DD} Supply Current	I_{DD}	μPD7811, 7810		1.5 *2	3.2	mA
		μPD78PG11E		1.5 *2	3.2	mA
V_{CC} Supply Current	I_{CC}	μPD7811,7810		150 *2	200	mA
		μPD78PG11E		140 *2	230	mA
Data Retention Voltage	V_{DDDR}	V_{CC} = 0V, RESET = V_{IL}	3.2			V

*2: T_a = 25°C, V_{CC} = V_{DD} = +5.0V

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≦ V_{DD} ≦ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		83	250	ns
Address Setup to ALE ↓	t_{AL}		65		ns
Address Hold from ALE ↓	t_{LA}		50		ns
Address to RD ↓ Delay Time	t_{AR}		150		ns
RD ↓ to Address Floating	t_{AFR}			20	ns
Address to Data Input	t_{AD}			360	ns
ALE ↓ to Data Input	t_{LDR}			215	ns
RD↓ to Data Input	t_{RD}			180	ns
ALE ↓ to RD ↓ Delay Time	t_{LR}		35		ns
Data Hold Time from RD ↑	t_{RDH}		0		ns
RD ↑ to ALE↑ Delay Time	t_{RL}		115		ns
RD Width Low	t_{RR}	Data Read	280		ns
		OP Code Fetch	530		ns
ALE Width High	t_{LL}		125		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}	*3, *6	65		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*3, *6	50		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*3, *7	65		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*3, *7	50		ns
Adress to WR ↓ Delay	t_{AW}		150		ns
ALE ↓ to Data Output	t_{LDW}			195	ns
WR ↓ to Data Output	t_{WD}			100	ns
ALE ↓ to WR ↓ Delay Time	t_{LW}		35		ns
Data Setup Time to WR ↑	t_{DW}		230		ns
Data Hold Time from WR ↑	t_{WDH}		95		ns
WR ↑ to ALE ↑ Delay Time	t_{WL}		115		ns
WR Width Low	t_{WW}		280		ns
Address to Data Input Delay	t_{ACC}	78PG11E only		360	ns

Note 1: f_{XTAL} = 10 MHz
2: Load Capacitance; C_L = 150pF

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*8	1.66		μs
			*9	500		ns
		$\overline{SCK}$ Output		2		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*8	750		ns
			*9	200		ns
		$\overline{SCK}$ Output		900		μs
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*8	750		ns
			*9	200		ns
		$\overline{SCK}$ Output		900		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*8		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*8		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*8			210	ns

*8: 1x Baud Rate in Asynchronous, Synchronous, I/O Interface Mode
*9: 16x Baud Rate or 64x Baud Rate in Asynchronous

ZERO-CROSS CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} −0.8V ≦ V_{DD} ≦ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

A/D CONVERTER CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = AV_{CC} = +5.0V ± 5 %, V_{SS} = AV_{SS} = 0V, AV_{CC} −0.5 ≤ V_{AREF} ≤ AV_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	Min	TYP		UNITS
Resolution			8			Bits
Absolute Accuracy		T_a = −10°C to +50°C 83ns ≤ t_{CYC} ≤ 170ns			0,4% ± 1/2	LSB
		83ns ≤ t_{CYC} ≤ 170ns			0.6% ± 1/2	LSB
Conversion Time	t_{CONV}	83ns ≤ t_{CYC} ≤ 110ns	576			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	432			t_{CYC}
Sampling Time	t_{SAMP}	83ns ≤ t_{CYC} ≤ 110ns	96			t_{CYC}
		110ns ≤ t_{CYC} ≤170ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}		0		V_{AREF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
V_{AREF} Current	I_{AREF}		0.2	0.5	1.5	mA

DC CHARACTERISTICS

(T_a = −40°C to +85°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1, X2	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1, X2 *1	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ V_{IN} ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) 0V ≤ V_{IN} ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	0.45V ≤ V_O ≤ V_{CC}			± 10	μA
AV_{CC} Supply Current	AI_{CC}			6	12	mA
V_{DD} Supply Current	I_{DD}	μPD7811, 7810		1.5 *2	3.5	mA
		μPD78PG11E		1.5 *2	3.5	mA
V_{CC} Supply Current	I_{CC}	μPD7811,7810		150 *2	220	mA
		μPD78PG11E		140 *2	250	mA
Data Retention Voltage	V_{DDDR}	V_{CC} = 0V, $\overline{RESET}$ = V_{IL}	3.2			V

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = −40°C to +85°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		100	250	ns
Address Setup to ALE ↓	t_{AL}		100		ns
Address Hold from ALE ↓	t_{LA}		70		ns
Address to RD ↓ Delay Time	t_{AR}		200		ns
RD ↑ to Address Floating	t_{AFR}			20	ns
Address to Data Input	t_{AD}			480	ns
ALE ↓ to Data Input	t_{LDR}			300	ns
RD↓ to Data Input	t_{RD}			250	ns
ALE ↓ to RD ↓ Delay Time	t_{LR}		50		ns
Data Hold Time from RD ↑	t_{RDH}		0		ns
RD ↑ to ALE↑ Delay Time	t_{RL}		150		ns
RD Width Low	t_{RR}	Data Read	350		ns
		OP Code Fetch	650		ns
ALE Width High	t_{LL}		160		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}	*6	100		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*6	70		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*7	100		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*7	70		ns
Adress to WR ↓ Delay	t_{AW}		200		ns
ALE ↓ to Data Output	t_{LDW}			210	ns
WR ↓ to Data Output	t_{WD}			100	ns
ALE ↓ to WR ↓ Delay Time	t_{LW}		50		ns
Data Setup Time to WR ↑	t_{DW}		300		ns
Data Hold Time from WR ↑	t_{WDH}		130		ns
WR ↑ to ALE ↑ Delay Time	t_{WL}		150		ns
WR Width Low	t_{WW}		350		ns
Address to Data Input Delay	t_{ACC}	78PG11E only		480	ns

Note 1: f_{XTAL} = 10 MHz

2: Load Capacitance; C_L = 150pF

SERIAL OPERATION

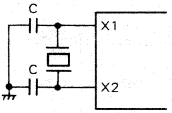
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*8	2.0		μs
			*9	500		ns
		$\overline{SCK}$ Output		2.4		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*8	920		ns
			*9	200		ns
		$\overline{SCK}$ Output		1.1		μs
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*8	920		ns
			*9	200		ns
		$\overline{SCK}$ Output		1.1		μs
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*8		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*8		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*8			210	ns

ZERO-CROSS CHARACTERISTICS

(T_a = −40°C to +85°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

*1 The following oscillation circuit using XTAL is recommended.



C=10 pF

*2 T_a = +25 °C, V_{CC} = V_{DD} = 5 V

*3 f_{XTAL} = 12 MHz

*4 f_{XTAL} = 10 MHz

*5 Load capacitance : C_L = 150 pF

*6 MODE0, MODE1 pins are connected to V_{CC} through R in μPD7810, μPD7811, μPD78PG11E

*7 MODE0, MODE1 pins are connected to V_{CC} through R in μPD7810

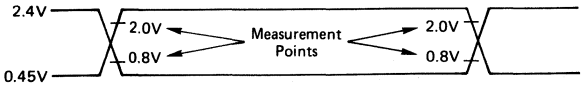
*8 1xBaud Rate in Asynchronous, Synchronous, I/O Interface Mode

*9 16x, 64x Baud Rate in Asynchronous

A/D CONVERTER CHARACTERISTICS

(t_a = −40°C to +85°C, V_{CC} = AV_{CC} = +5.0V ± 10%, V_{SS} = AV_{SS} = 0V, AV_{CC} −0.5V ≦ V_{AREF} ≦ AV_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	Min	TYP		UNITS
Resolution			8			Bits
Absolute Accuracy		T_a = −10°C to +50°C 100ns ≦ t_{CYC} ≦ 170ns			0.4% ± 1/2	LSB
		100ns ≦ t_{CYC} ≦ 170ns			0.6% ± 1/2	LSB
Conversion Time	t_{CONV}	100ns ≦ t_{CYC} ≦ 170ns	576			t_{CYC}
		110ns ≦ t_{CYC} ≦ 170ns	432			t_{CYC}
Sampling Time	t_{SAMP}	100ns ≦ t_{CYC} ≦ 110ns	96			t_{CYC}
		110ns ≦ t_{CYC} ≦170ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}		0		V_{AREF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
V_{AREF} Current	I_{AREF}		0.2	0.5	1.5	mA



AC TIMING MEASUREMENT POINT

BUS TIMING DEPENDING ON t_{CYC}

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNITS
t_{AL}	2T − 100	MIN	ns
t_{LA}	T − 30	MIN	ns
t_{AR}	3T − 100	MIN	ns
t_{AD}	7T − 220	MAX	ns
t_{LDR}	5T − 200	MAX	ns
t_{RD}	4T − 150	MAX	ns
t_{LR}	T − 50	MIN	ns
t_{RL}	2T − 50	MIN	ns
t_{RR}	4T − 50 (Data Read)	MIN	ns
	7T − 50 (OP Code Fetch)		
t_{LL}	2T − 40	MIN	ns
t_{ML} *2	2T − 100	MIN.	ns
t_{LM} *2	T − 30	MIN.	ns
t_{IL} *3	2T − 100	MIN.	ns
t_{LI} *3	T − 30	MIN.	ns
t_{AW}	3T − 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T − 50	MIN	ns
t_{DW}	4T − 100	MIN	ns
t_{WDH}	2T − 70	MIN	ns
t_{WL}	2T − 50	MIN	ns
t_{WW}	4T − 50	MIN	ns
t_{CYK}	20T ($\overline{SCK}$ Input) *1	MIN	ns
	24T ($\overline{SCK}$ Output)		
t_{KKL}	10T − 80 ($\overline{SCK}$ Input) *1	MIN	ns
	12T − 100 ($\overline{SCK}$ Output)		
t_{KKH}	10T − 80 ($\overline{SCK}$ Input) *1	MIN	ns
	12T − 100 ($\overline{SCK}$ Output)		

*1: 1x Baud Rate in Asynchronous, Synchronous, I/O Interface Mode.
*2: MODE0, MODE1 pins are connected to V_{CC} through R.
*3: MODE0, MODE1 pins are connected to V_{CC} through R in μPD7810.

Note: T = t_{CYC} = $1/f_{XTAL}$

OTHER OPERATIONS

(T_a = −10°C to +70°C, V_{CC} = +5.0V± 5%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})
(T_a = −40°C to + 85°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0,8V ≤ V_{DD} ≤ V_{CC})

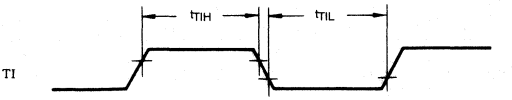
Parameter	Symbol	Conditions	MIN	MAX	UNITS
TI width high, low	t_{TIH}, t_{TIL}		6		t_{CYC}
CI width high, low	t_{CI1H}, t_{CI1L}	Event Count Mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	Pulse Width Measurement Mode	48		t_{CYC}
$\overline{NMI}$ width high, low	t_{NIH}, t_{NIL}		36		t_{CYC}
INT1 width high, low	t_{I1H}, t_{I1I}		36		t_{CYC}
$\overline{INT2}$ width high, low	t_{I2H}, t_{I2L}		36		t_{CYC}
$\overline{RESET}$ width high, low	t_{RSH}, t_{RSL}		60		t_{CYC}

EXTERNAL CLOCK TIMING

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5%, V_{SS} =0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})
(T_a = −40°C to + 85°C, V_{CC} = + 5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

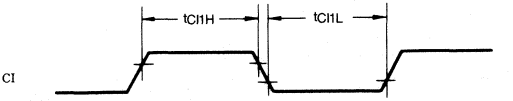
Parameter	Symbol	Twst Conditions	MIN	MAX	UNITS
X1 input width high	$t_{ØH}$		30	250	ns
X1 input width low	$t_{ØL}$		30	250	ns
X1 input rise time	t_r		0	30	ns
X1 input fall time	t_f		0	30	ns

TIMER INPUT TIMING

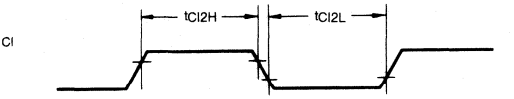


TIMER/EVENT COUNTER INPUT TIMING

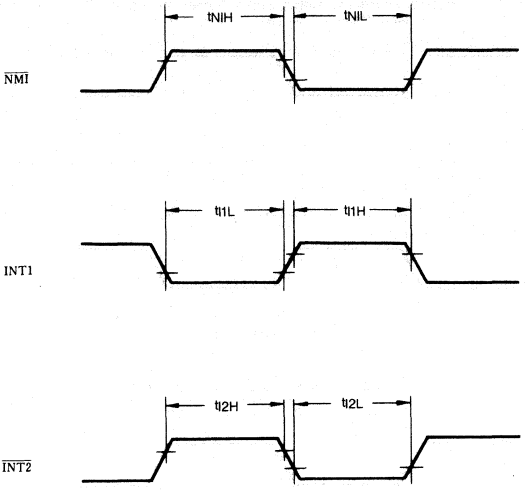
EVENT COUNT MODE



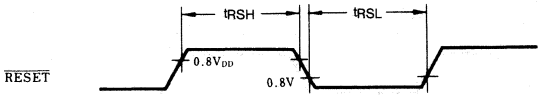
PULSE WIDTH MEASUREMENT MODE



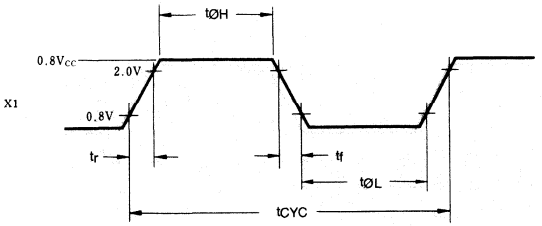
INTERRUPT INPUT TIMING



RESET INPUT TIMING



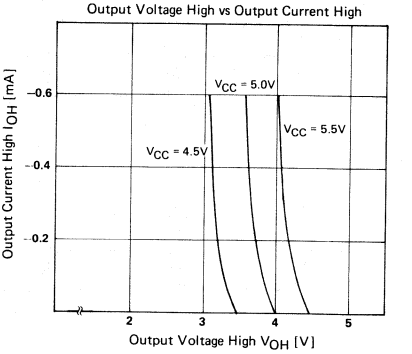
EXTERNAL CLOCK TIMING



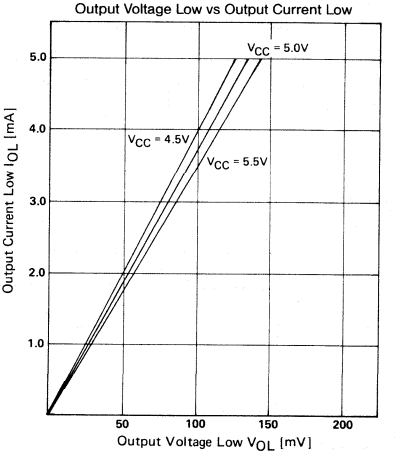
CHARACTERISTICS CURVE
— REFERENCE —

(T_a = 25°C)

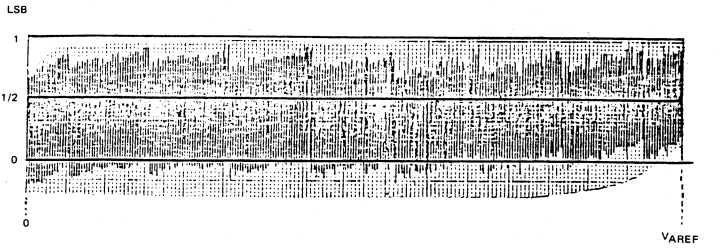
Output Voltage High vs Output Current High



Output Voltage Low vs Output Current Low

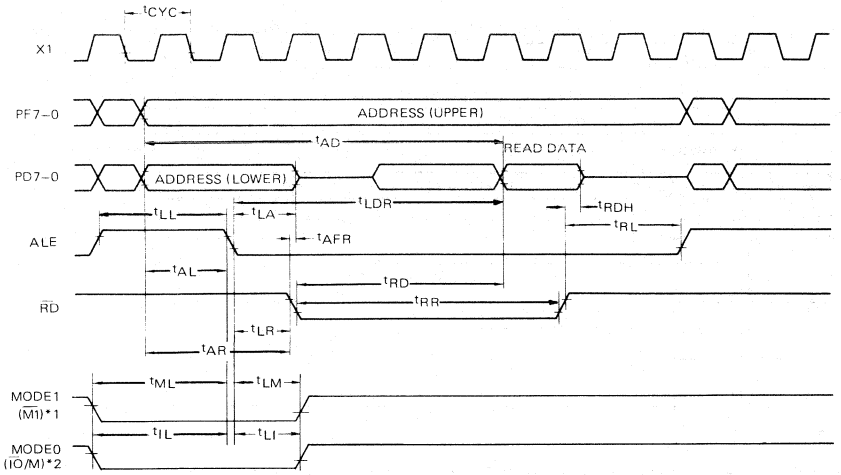


CHARACTERISTIC OF A/D CONVERTER



TIMING WAVEFORM

Read Operation

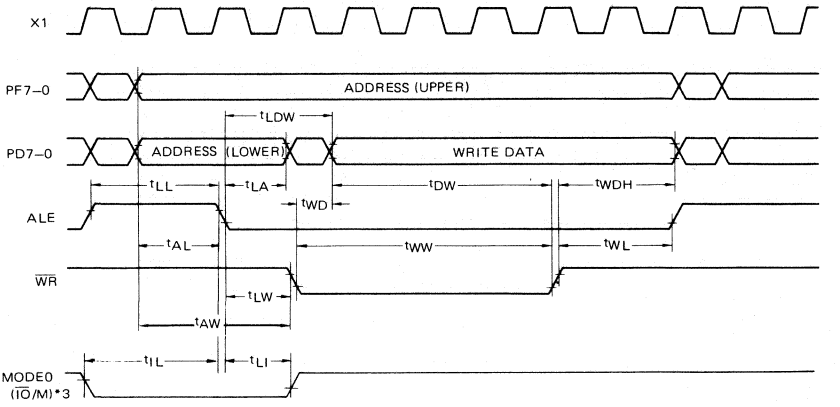


*1 $\overline{M1}$ is output at the fetch cycle of the 1st byte of the instruction in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

*2 $\overline{IO}$/M is output only when registers (sr-sr2) are read in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

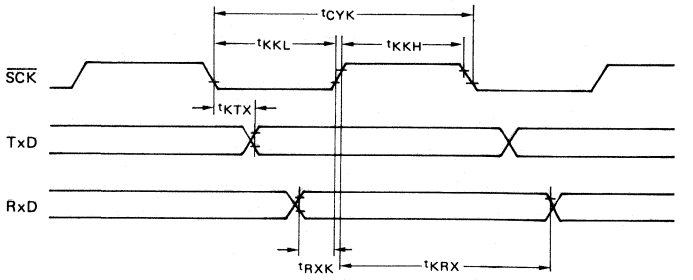
TIMING WAVEFORM

Write Operation

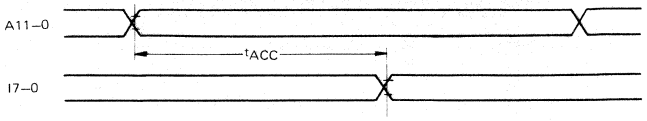


*3 IO/M is output only when registers (sr-sr2) are written in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

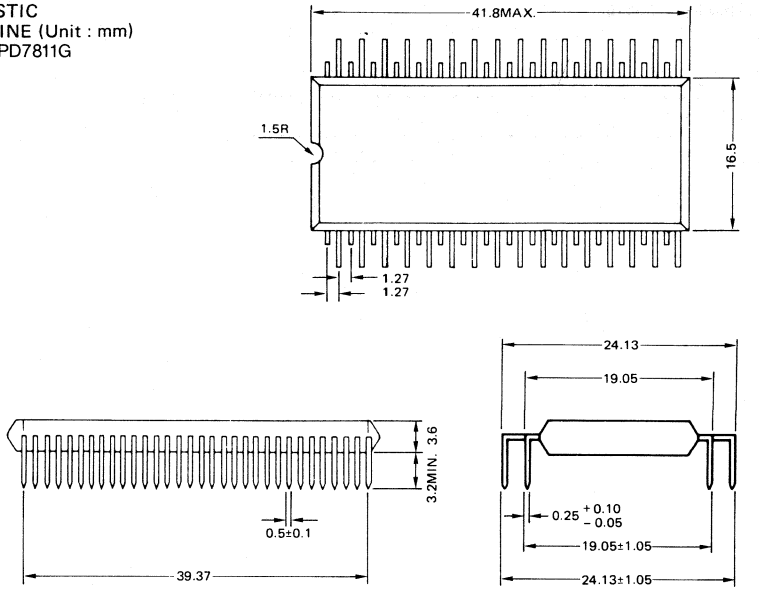
Serial Operation



EPROM Timing (for μPD78PG11E)

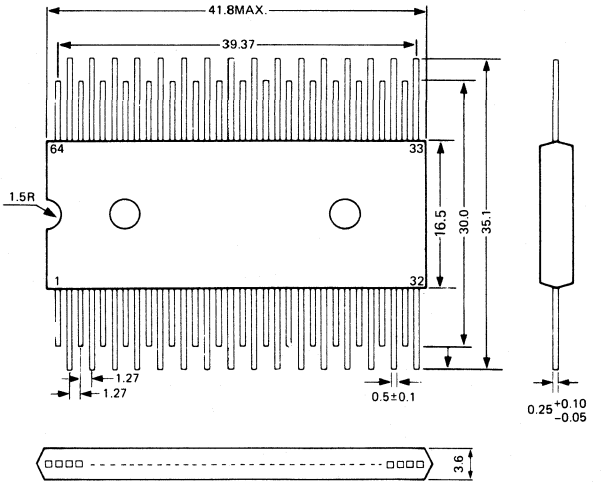


64 PIN PLASTIC
QUIP OUTLINE (Unit : mm)
μPD7801G/μPD7811G



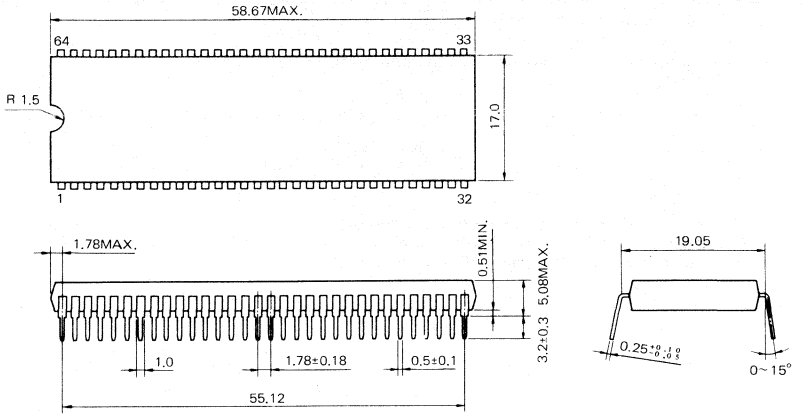
When ordering this package, specify as follows:
μPD7810G-36
μPD7811G-xxx-36

64 PIN PLASTIC QUIP OUTLINE
FLAT LEADS
(Unit : mm)
μPD7811G



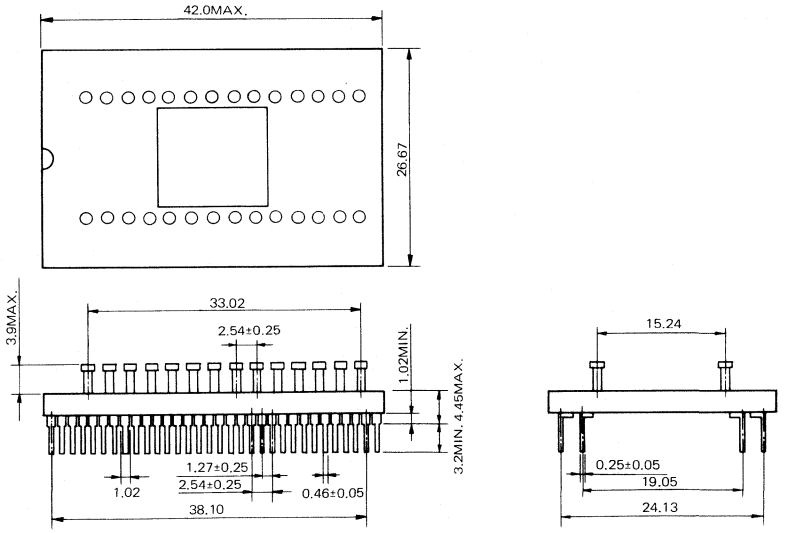
When ordering this package, specify as follows: μPD7811G-XXX-37

64 PIN PLASTIC
SHRINK DIP OUTLINE (Unit : mm)
μPD 7810CW/μPD7811CW

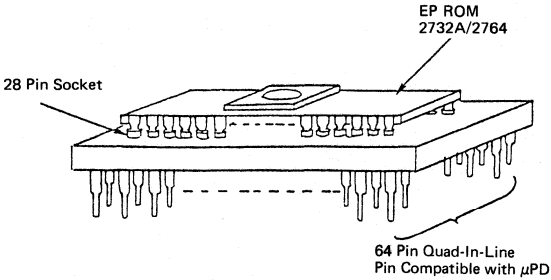


When ordering this package, specify as follows:
μPD7810CW
μPD7811CW-xxx

64 PIN CERAMIC
PIGGY BACK QUIP OUTLINE (Unit : mm)
μPD78PG11E



QUIL CERAMIC PIGGY BACK
PACKAGE OUTLINE
μPD78PG11E



- μPD78PG11E can access eprom when addressing 0 to 4095
- All memory of the 2732A memory (4K-Byte memory)
- Lower 4K-Byte of the 2764 memory (8K-Byte memory)

PRELIMINARY

ELECTRICAL SPECIFICATIONS

AND PACKAGE OUTLINES FOR

μPD7810H/7811H

ABSOLUTE MAXIMUM RATINGS

(T_a = 25° C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power Supply Voltage	V_{CC}		−0.5 to +7.0	V
	V_{DD}		−0.5 to +7.0	V
	AV_{CC}		−0.5 to +7.0	V
	AV_{SS}		−0.5 to +0.5	V
Input Voltage	V_I		−0.5 to +7.0	V
Output Voltage	V_O		−0.5 to + 7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−0.5	mA
		All Output Pin Total	−20	mA
Reference Input Voltage	V_{AREF}		−0.5 to V_{CC}	V
Operating Temperature	T_{opt}	$f_{XTAL} \leq 15$ MHz	−10 to +70	°C
Storage Temperature	T_{stg}		−65 to +150	°C

OPERATING CONDITION

OSC. FREQ. \ PARAMETER	T_a	V_{CC}, AV_{CC}
$f_{XTAL} \leq 15$ MHz	−10°C to +70°C	+5.0V ± 10 %

CAPACITANCE

(T_a= 25°C, $V_{CC} = V_{DD} = V_{SS} = 0V$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_c = 1 MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	$C_{I/O}$				20	pF

DC CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ V_I ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) 0V ≤ V_I ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	0.45V≤V_O≤V_{CC}			± 10	μA
AV_{CC} Supply Current	AI_{CC}			6	12	mA
V_{DD} Supply Current	I_{DD}			1.5 *1	3.2	mA
V_{CC} Supply Current	I_{CC}			150 *1	200	mA
Data Retention Voltage	V_{DDDR}	$V_{CC} = 0$, $\overline{RESET} = V_{IL}$	3.2			V

*1: T_a = 25°C, $V_{CC} = V_{DD}$ = +5.0V

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		66	250	ns
Address Setup to ALE ↓	t_{AL}		30		ns
Address Hold from ALE ↓	t_{LA}		35		ns
Address to RD ↓Delay Time	t_{AR}		100		ns
RD ↓to Address Floating	t_{AFR}			20	ns
Address to Data Input	t_{AD}			250	ns
ALE ↓to Data Input	t_{LDR}			135	ns
RD↓to Data Input	t_{RD}			120	ns
ALE ↓to RD ↓Delay Time	t_{LR}		15		ns
Data Hold Time from RD ↑	t_{RDH}		0		ns
RD ↑ to ALE↑ Delay Time	t_{RL}		80		ns
RD Width Low	t_{RR}	Data Read	215		ns
		OP Code Fetch	415		ns
ALE Width High	t_{LL}		90		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}		30		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}		35		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}		30		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}		35		ns
Adress to WR ↓Delay	t_{AW}		100		ns
ALE ↓to Data Output	t_{LDW}			180	ns
WR ↓to Data Output	t_{WD}			100	ns
ALE ↓to WR ↓Delay Time	t_{LW}		15		ns
Data Setup Time to WR ↑	t_{DW}		165		ns
Data Hold Time from WR ↑	t_{WDH}		60		ns
WR ↑to ALE ↑Delay Time	t_{WL}		80		ns
WR Width Low	t_{WW}		215		ns

Note 1: f_{XTAL} = 12 MHz
2: Load Capacitance; C_L = 150pF

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*2	800		ns
			*3	500		ns
		$\overline{SCK}$ Output		1.6		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*2	335		ns
			*3	200		ns
		$\overline{SCK}$ Output		700		μs
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*2	335		ns
			*3	200		ns
		$\overline{SCK}$ Output		700		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*2		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*2		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*2			210	ns

*2: 1x Baud Rate in Asynchronous, Synchronous, I/O Interface Mode
*3: 16x Baud Rate or 64x Baud Rate in Asynchronous

ZERO-CROSS CHARACTERISTICS

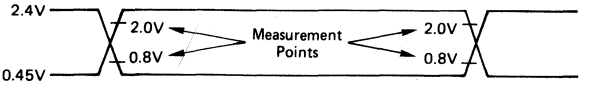
(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

A/D CONVERTER CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = AV_{CC} = +5.0V ±10%, V_{SS} = AV_{SS} = 0V, AV_{CC} −0.5 ≤ V_{AREF} ≤ AV_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	Min	TYP		UNITS
Resolution			8			Bits
Absolute Accuracy		T_a = 0°C to +70°C, 66ns ≤ t_{CYC} ≤ 170ns			0.4% ± 1/2	LSB
Conversion Time	t_{CONV}	66ns ≤ t_{CYC} ≤ 110ns	576			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	432			t_{CYC}
Sampling Time	t_{SAMP}	66ns ≤ t_{CYC} ≤ 110ns	96			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}		0		V_{AREF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
V_{AREF} Current	I_{AREF}		0.1	2.0	5.0	mA



AC TIMING MEASUREMENT POINT

BUS TIMING DEPENDING ON t_{CYC}

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNITS
t_{AL}	2T − 100	MIN	ns
t_{LA}	T − 30	MIN	ns
t_{AR}	3T − 100	MIN	ns
t_{AD}	7T − 220	MAX	ns
t_{LDR}	5T − 200	MAX	ns
t_{RD}	4T − 150	MAX	ns
t_{LR}	T − 50	MIN	ns
t_{RL}	2T − 50	MIN	ns
t_{RR}	4T − 50 (Data Read)	MIN	ns
	7T − 50 (OP Code Fetch)		
t_{LL}	2T − 40	MIN	ns
t_{ML} *2	2T − 100	MIN.	ns
t_{LM} *2	T − 30	MIN.	ns
t_{IL} *3	2T − 100	MIN.	ns
t_{LI} *3	T − 30	MIN.	ns
t_{AW}	3T − 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T − 50	MIN	ns
t_{DW}	4T − 100	MIN	ns
t_{WDH}	2T − 70	MIN	ns
t_{WL}	2T − 50	MIN	ns
t_{WW}	4T − 50	MIN	ns
t_{CYK}	12T ($\overline{SCK}$ Input) *1	MIN	ns
	24T ($\overline{SCK}$ Output)		
t_{KKL}	5T + 5 ($\overline{SCK}$ Input) *1	MIN	ns
	12T − 100 ($\overline{SCK}$ Output)		
t_{KKH}	5T + 5 ($\overline{SCK}$ Input) *1	MIN	ns
	12T − 100 ($\overline{SCK}$ Output)		

*1: 1x Baud Rate in Asynchronous, Synchronous, I/O Interface Mode.

Note 1: T = t_{CYC} = 1/f_{XTAL}

2: The items out of this table are not dependent on f_{XTAL}.

OTHER OPERATIONS

(T_a = −10°C to + 70°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

Parameter	Symbol	Conditions	MIN	MAX	UNITS
TI width high, low	t_{TIH}, t_{TIL}		6		t_{CYC}
CI width high, low	t_{CI1H}, t_{CI1L}	Event Count Mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	Pulse Width Measurement Mode	48		t_{CYC}
$\overline{NMI}$ width high, low	t_{NIH}, t_{NIL}		36		t_{CYC}
INT1 width high, low	t_{I1H}, t_{I1L}		36		t_{CYC}
$\overline{INT2}$ width high, low	t_{I2H}, t_{I2L}		36		t_{CYC}
$\overline{RESET}$ width high, low	t_{RSH}, t_{RSL}		60		t_{CYC}

EXTERNAL CLOCK TIMING

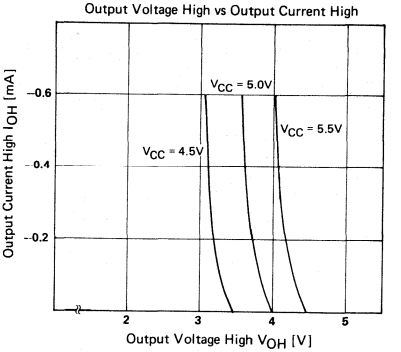
(T_a = −10°C to + 70°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

Parameter	Symbol	Test Condition	MIN	MAX	UNITS
X1 input width high	$t_{\phi H}$		20	250	ns
X1 input width low	$t_{\phi L}$		20	250	ns
X1 input rise time	t_r		0	20	ns
X1 input fall time	t_f		0	20	ns

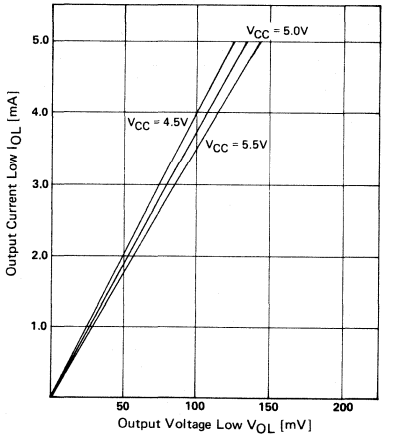
CHARACTERISTICS CURVE
– REFERENCE –

(T_a = 25°C)

Output Voltage High vs Output Current High

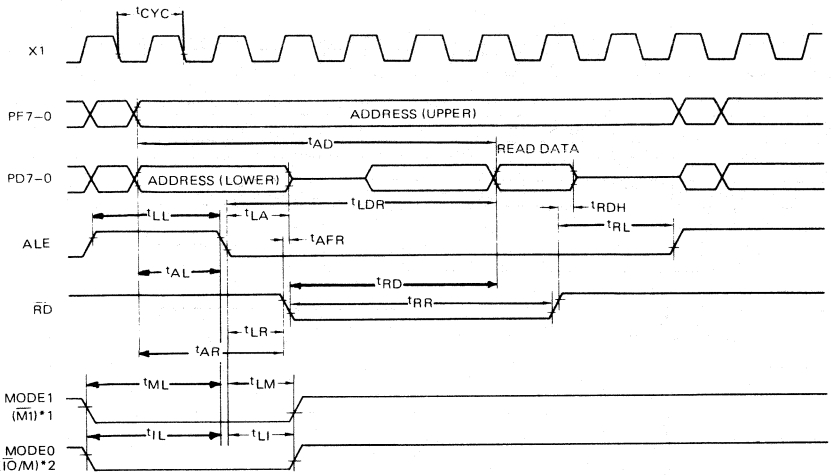


Output Voltage Low vs output Current Low



TIMING WAVEFORM

Read Operation

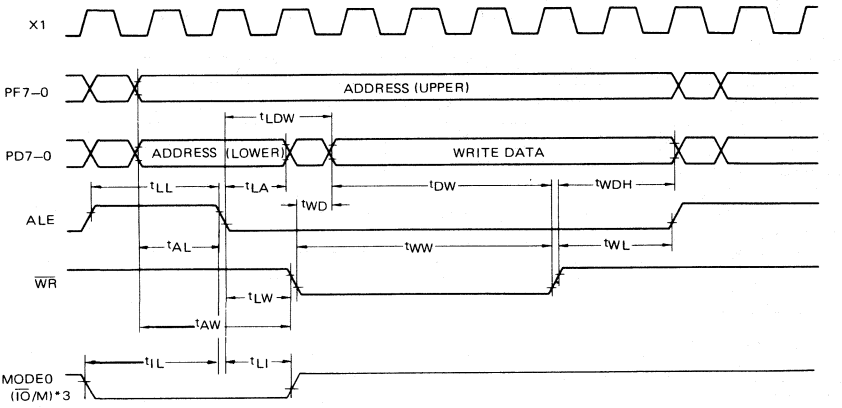


*1 $\overline{M1}$ is output at the fetch cycle of the 1st byte of the instruction in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

*2 $\overline{IO}$/M is output only when registers (sr-sr2) are read in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

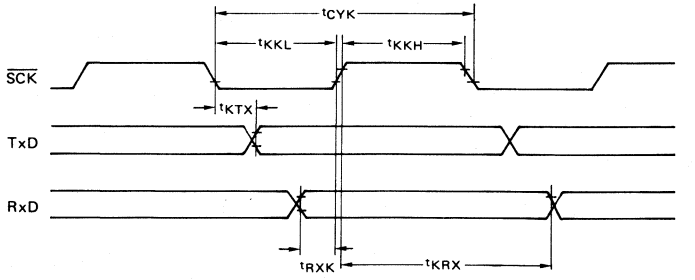
TIMING WAVEFORM

Write Operation

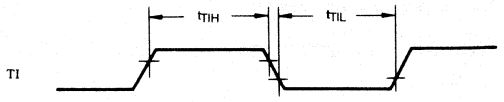


*3 $\overline{IO}$/M is output only when registers (sr-sr2) are written in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

Serial Operation

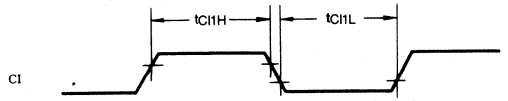


TIMER INPUT TIMING

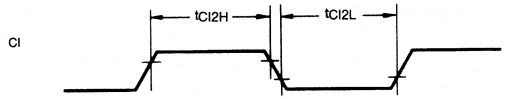


TIMER/EVENT COUNTER INPUT TIMING

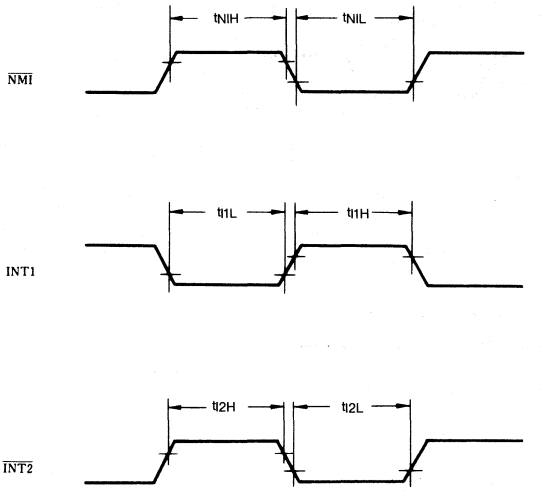
EVENT COUNT MODE



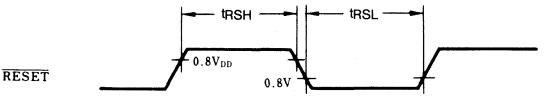
PULSE WIDTH MEASUREMENT MODE



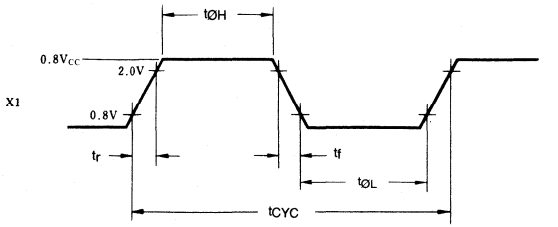
INTERRUPT INPUT TIMING



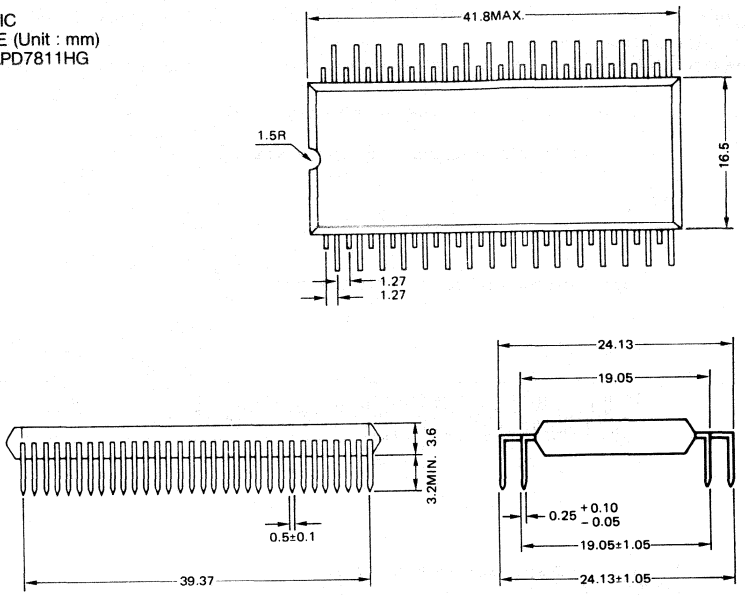
RESET INPUT TIMING



EXTERNAL CLOCK TIMING

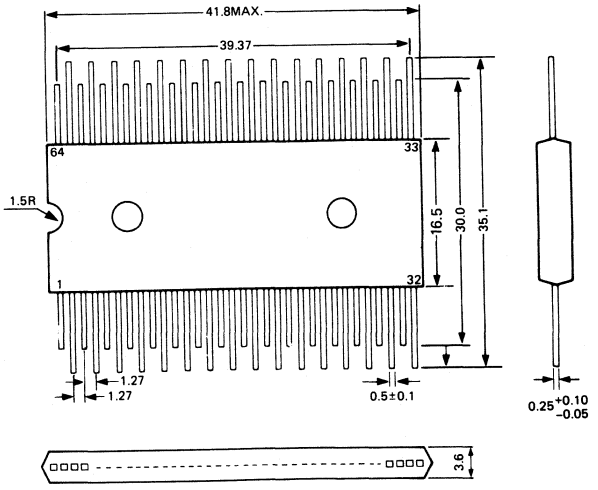


64 PIN PLASTIC
QUIP OUTLINE (Unit : mm)
μPD7810HG/μPD7811HG



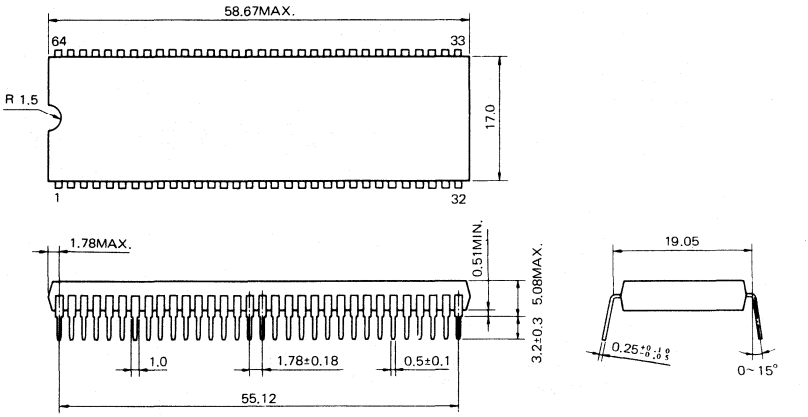
When ordering this package, specify as follows:
μPD7810HG-36
μPD7811HG-xxx-36

64 PIN PLASTIC
QUIP PACKAGE OUTLINE
(Unit : mm)
μPD7811HG



When ordering this package, specify as follows: μPD7811HG-XXX-37

64 PIN PLASTIC
SHRINK DIP OUTLINE (Unit : mm)
μPD7810HCW/μPD7811HCW



When ordering this package, specify as follows:
μPD7810HCW
μPD7811HCW-xxx

PRELIMINARY

ELECTRICAL SPECIFICATIONS

AND PACKAGE OUTLINES FOR

μPD78C10/78C11/78C14*

* Note: For μPD78C14 this specification is only target and some parameters, especially DC Characteristics and Absolute Ratings, may change without notice

ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C)

Parameter	Symbol	Test Condition	Ratings	Unit
Power Supply Voltage	V_{DD}		−0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD} + 0.5	V
	AV_{SS}		−0.5 to +0.5	V
Input Voltage	V_I		−0.5 to V_{DD} +0.5	V
Output Voltage	V_O		−0.5 to V_{DD} +0.5	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−2.0	mA
		All Output Pin Total	−50	mA
Reference Input Voltage	V_{AREF}		−0.5 to AV_{DD} +0.3	V
Operating Temperature	T_{opt}	$f_{XTAL} \leq$ 12MHz	−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

OPERATING CONDITION

OSC frequency \ Parameter	Ta	V_{DD}, AV_{DD}
$f_{XTAL} \leq$ 12MHz	−40°C to +85°C	+5.0V ± 10%

CAPACITANCE

(T_a = 25°C, V_{DD} = V_{SS} = 0V)

Paramater	Symbol	Test Condition	MIN	TYP	MAX	UNIT
Input Capacitance	C_I	f_C = 1MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	C_{IO}				20	pF

(T_a = -40°C to +85°C, V_{DD} = +5.0V±10%, V_{SS} = 0V)

DC CHARACTERISTICS

Parameter	Symbol	Test Condition	MIN	TYP	MAX	UNIT
Input Low Voltage	V_{IL1}	All except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT 1, TI, AN4 to 7	0		0.8	V
	V_{IL2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN4 to 7	0		$0.2V_{DD}$	V
Input High Voltage	V_{IH1}	All except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN4 to 7, X1, X2	2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN4 to 7, X1, X2	$0.8V_{DD}$		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA	V_{DD}-1.0			V
		I_{OH} = -100μA	V_{DD}-0.5			V
Input Current	I_I	INT1, TI (PC3); $0V \leqq V_I \leqq V_{DD}$			±200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3), $0V \leqq V_I \leqq V_{DD}$			±10	μA
Output Leakage Current	I_{LO}	$0V \leqq V_O \leqq V_{DD}$			±10	μA
AV_{DD} Supply Current	AI_{DD}			0.3	1.0	mA
V_{DD} Supply Current	I_{DD1}	Operation mode f=12MHz		15	30	mA
	I_{DD2}	HALT MODE f=12MHz		10	20	mA
Data Retention Voltage	V_{DDDR}	Hardware/Software STOP MODE	2.5			V
Data Retention Current	I_{DDDR}	Hardware/Software STOP Mode, V_{DDDR} = 2,5V		1	15	μA
		V_{DDDR} = 5V±10%		10	50	μA

AC CHARACTERISTICS (T_a = -40°C to +85°C, V_{DD} = + 5.0 V ± 10%, V_{SS} = 0V)

READ/WRITE OPERATION

Parameter	Symbol	Test Condition	MIN	MAX	Unit
X1 Input Cycle Time	t_{CYC}		83	250	ns
Address Setup to ALE↓	t_{AL}	*3, *4	65		ns
Adress Hold after ALE↓	t_{LA}	*3, *4	50		ns
Adress to $\overline{RD}$↓ Delay Time	t_{AR}	*3, *4	150		ns
$\overline{RD}$↓ to Address Floating	t_{AFR}	*4		20	ns
Adress to Data Input	t_{AD}	*3, *4		360	ns
ALE↓ to Data Input	t_{LDR}	*3, *4		215	ns
$\overline{RD}$↓ to Data Input	t_{RD}	*3, *4		180	ns
ALE to $\overline{RD}$↓ Delay Time	t_{LR}	*3, *4	35		ns
Data Hold after $\overline{RD}$↑	t_{RDH}	*4	0		ns
$\overline{RD}$↑ to ALE↑ Delay Time	t_{RL}	*3, *4	115		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read, *3, *4	280		ns
		OP code Fetch, *3, *4	530		ns
ALE Width High	t_{LL}	*3, *4	125		ns
$\overline{M1}$ Setup time to ALE↓	t_{ML}	*3	65		ns
$\overline{M1}$ Hold Time after ALE↓	t_{LM}	*3	50		ns
$\overline{IO}$/M Setup Time to ALE↓	t_{IL}	*3	65		ns
$\overline{IO}$/M Hold Time after ALE↓	t_{LI}	*3	50		ns
Address to $\overline{WR}$↓ Delay	t_{AW}	*3, *4	150		ns
ALE↓ to Data Output	t_{LDW}	*3, *4		195	ns
$\overline{WR}$↓ to Data Output	t_{WD}	*4		100	ns
ALE to $\overline{WR}$↓ Delay	t_{LW}	*3, *4	35		ns
Data Setup Time to $\overline{WR}$↑	t_{DW}	*3, *4	230		ns
Data Hold Time after $\overline{WR}$↑	t_{WDH}	*3, *4	95		ns
$\overline{WR}$↑ to ALE ↑ Delay Time	t_{WL}	*3, *4	115		ns
$\overline{WR}$ Width Low	t_{WW}	*3, *4	280		ns

AC CHARACTERISTICS
SERIAL OPERATION

Parameter	Symbol	Test Condition		MIN	MAX	UNIT
$\overline{SCK}$ Cycle Time	tCYK	$\overline{SCK}$ Input	*5	1		μs
			*6	500		ns
		$\overline{SCK}$ Output		2		μs
$\overline{SCK}$ Width Low	tKKL	$\overline{SCK}$ Input	*5	420		ns
			*6	200		ns
		$\overline{SCK}$ Output		900		ns
$\overline{SCK}$ Width High	tKKH	$\overline{SCK}$ Input	*5	420		ns
			*6	200		ns
		$\overline{SCK}$ Output		900		ns
RxD Setup Time to $\overline{SCK}$↑	tRXK	*5		80		ns
RxD Hold Time After $\overline{SCK}$↑	tKRX	*5		80		ns
$\overline{SCK}$↓ to TxD Delay Time	tKTX	*5			210	ns

(T_a = -40°C to +85°C, V_{DD} = +5.0V ± 10%, V_{SS} = AV_{SS} = 0V, V_{DD} -0.5V ≦ AV_{DD} ≦ V_{DD}, 4.0V ≦ V_{AREF} ≦ AV_{DD})

A/D CONVERTER
CHARACTERISTICS

Parameter	Symbol	Test Condition	MIN	TYP	MAX	UNIT
Resolution			8			Bits
Absolute Accuracy		Ta = -10°C to +50°C, 83ns ≦ t_{CYC} ≦ 170ns			0.4%±1/2	LSB
		83ns ≦ t_{CYC} ≦ 170ns			0.6%±1/2	LSB
		3.4V ≦ V_{AREF} ≦ AV_{DD} 83ns ≦ t_{CYC} ≦ 170ns			0.8%±1/2	LSB
Conversion time	tCONV	83ns ≦ t_{CYC} ≦ 110ns	576			t_{CYC}
		110ns ≦ t_{CYC} ≦ 170ns	432			t_{CYC}
Sampling Time	tSAMP	83ns ≦ t_{CYC} ≦ 110ns	96			t_{CYC}
		110ns ≦ t_{CYC} ≦ 170ns	72			t_{CYC}
Analog Input Voltage	VIAN		0		V_{AREF}	V
Analog Input Impedance	RAN			1000		MΩ
V_{AREF} Current	IAREF			1.5	3.0	mA

ZERO-CROSS CHARACTERISTICS

(T_a = -40°C to +85°C, V_{DD} = +5.0V±10%, V_{SS} = 0V)

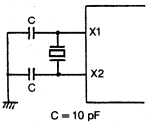
Parameter	Symbol	Test Condition	MIN	MAX	UNIT
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60Hz Sine Wave		±135	mV
Zero-Cross Detection Input Frequency	f_{ZX}		0.05	1	kHz

OTHER OPERATIONS

(T_a = -40°C to +85°C, V_{DD} = +5.0V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Condition	MIN	MAX	UNIT
TI width high, low	t_{TIH}, t_{TIL}		6		t_{CYC}
CI width high, low	t_{CI1H}, t_{CI1L}	Event Count Mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	Pulse Width Measurement Mode	48		t_{CYC}
$\overline{NMI}$ width high, low	t_{NIH}, t_{NIL}		10		μs
INT1 width high, low	t_{I1H}, t_{I1L}		36		t_{CYC}
$\overline{INT2}$ width high, low	t_{I2H}, t_{I2L}		36		t_{CYC}
$\overline{RESET}$ width high, low	t_{RSH}, t_{RSL}		10		μs

*1. For XTAL oscillation, following circuit is recommended.



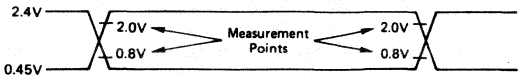
*2. T_a = +25°C, V_{DD} = 5 V

*3. f_{XTAL} = 12MHz

*4. Load Capacitance: C_L = 150pF

*5. x1 Clock Rate in Asynchronous Mode, Synchronous Mode, I/O Interface Mode

*6. x16, x64 Clock Rate in Asynchronous Mode



AC TIMING
MEASUREMENT POINT

EXTERNAL CLOCK
TIMING

(T_a = −40°C to +85°C, V_{DD} = +5.0V ± 10%)

Parameter	Symbol	Test Condition	MIN	MAX	UNIT
X1 input width high	tØH		30	250	ns
X1 input width low	tØL		30	250	ns
X1 input rise time	t_r		0	30	ns
X1 input fall time	t_f		0	30	ns

BUS TIMING
DEPENDING ON t_{CYC}

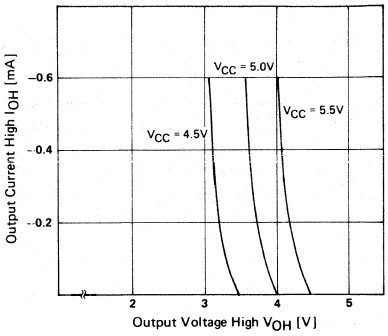
Symbol	Calculating Expression	MIN./MAX.	units
t_{AL}	2T – 100	MIN	ns
t_{LA}	T – 30	MIN	ns
t_{AR}	3T – 100	MIN	ns
t_{AD}	7T – 220	MAX	ns
t_{LDR}	5T – 200	MAX	ns
t_{RD}	4T – 150	MAX	ns
t_{LR}	T – 50	MIN	ns
t_{RL}	2T – 50	MIN	ns
t_{RR}	4T – 50 (Data Read)	MIN	ns
	7T – 50 (OP Code Fetch)		
t_{LL}	2T – 40	MIN	ns
t_{ML}	2T – 100	MIN	ns
t_{LM}	T – 30	MIN	ns
t_{IL}	2T – 100	MIN	ns
t_{LI}	T – 30	MIN	ns
t_{AW}	3T – 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T – 50	MIN	ns
t_{DW}	4T – 100	MIN	ns
t_{WDH}	2T – 70	MIN	ns
t_{WL}	2T – 50	MIN	ns
t_{WW}	4T – 50	MIN	ns
t_{CYK}	12T ($\overline{SCK}$ Input) *1	MIN	ns
	24T ($\overline{SCK}$ Output)		
t_{KKL}	5T + 5 ($\overline{SCK}$ Input) *1	MIN	ns
	12T – 100 ($\overline{SCK}$ Output)		
t_{KKH}	5T + 5 ($\overline{SCK}$ Input) *2	MIN	ns
	12T – 100 ($\overline{SCK}$ Output)		

Note 1. In case of x1 clock rate in asynchronous mode, synchronous mode, or I/O interface mode.
2. $T = t_{CYC} = 1/f_{XTAL}$
3. Parameters which can't be found in this table don't depend on oscillation frequency (f_{XTAL}).

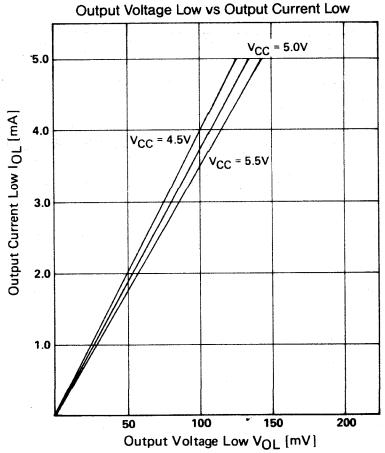
CHARACTERISTICS CURVE
– REFERENCE –

(T_a = 25°C)

Output Voltage High vs Output Current High

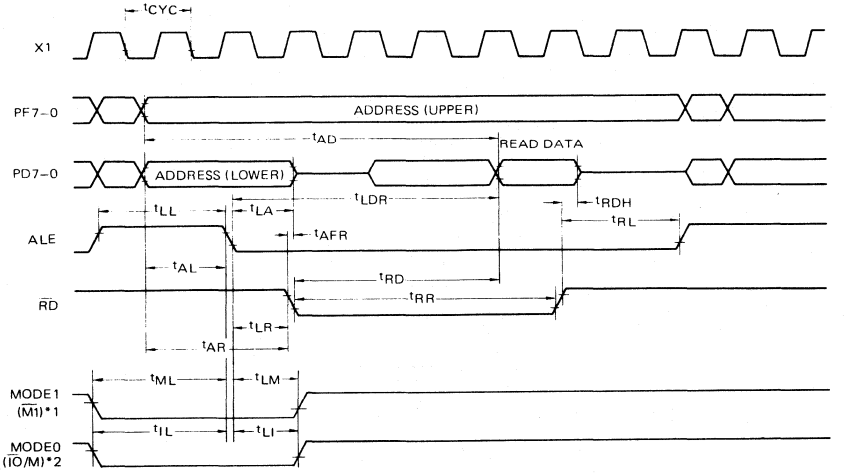


Output Voltage Low vs Output Current Low



TIMING WAVEFORM

Read Operation

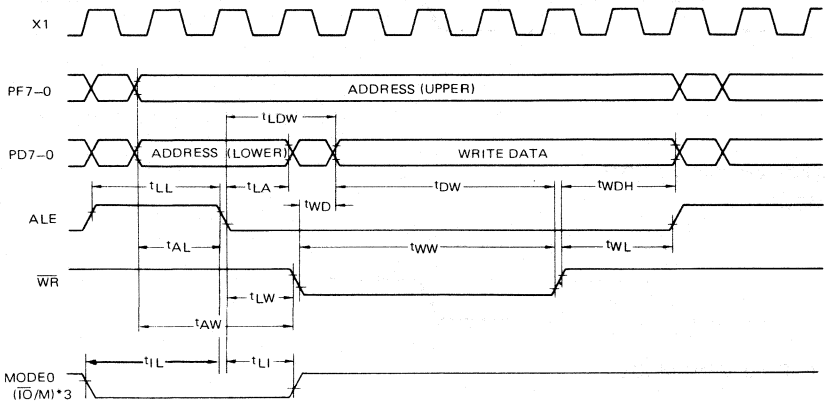


*1 $\overline{M_1}$ is output at the fetech cycle of the 1st byte of the instruction in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

*2 $\overline{IO}$/M is output only when registers (sr-sr2) are read in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

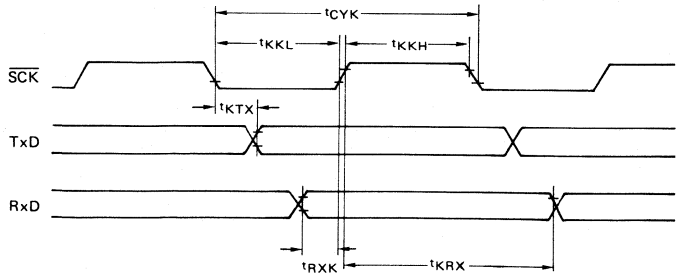
TIMING WAVEFORM

Write Operation

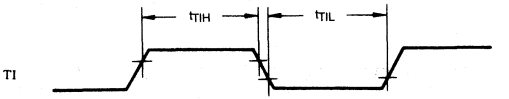


*3 $\overline{IO}$/M is output only when registers (sr-sr2) are written in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

Serial Operation

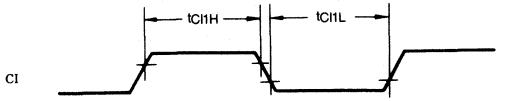


TIMER INPUT TIMING

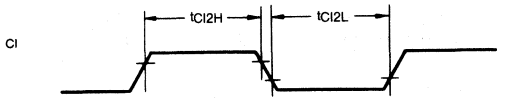


TIMER/EVENT COUNTER INPUT TIMING

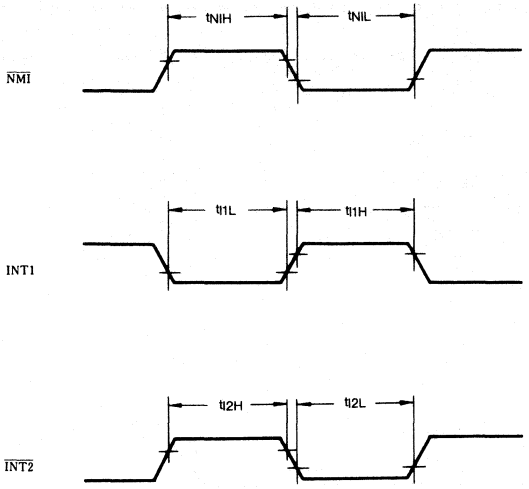
EVENT COUNT MODE



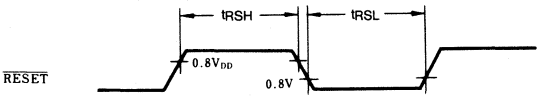
PULSE WIDTH MEASUREMENT MODE



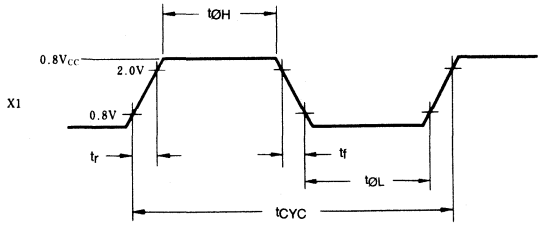
INTERRUPT INPUT TIMING



RESET INPUT TIMING



EXTERNAL CLOCK TIMING

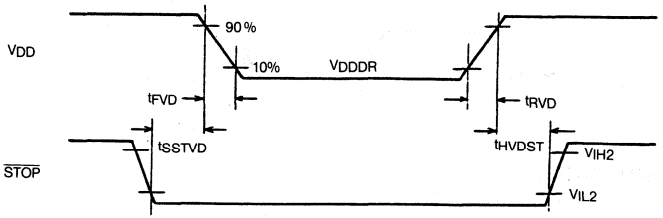


DATA MEMORY STOP MODE DATA RETENTION CHARACTERISTICS

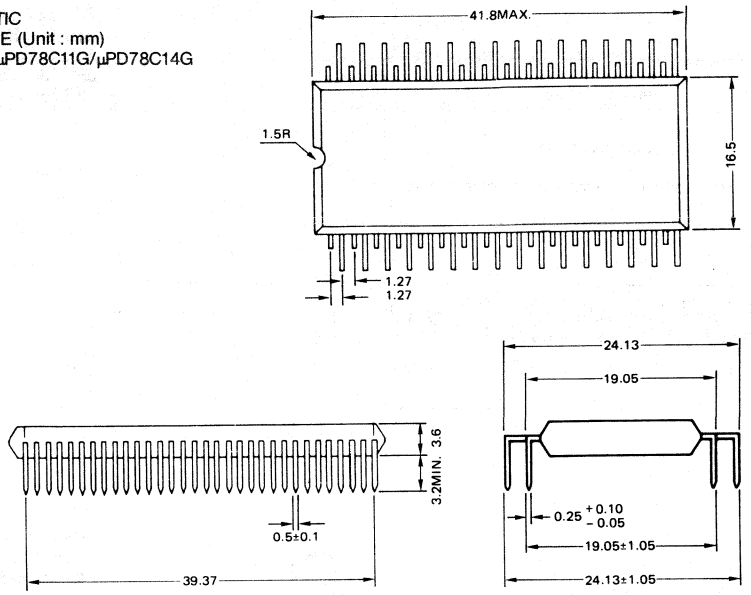
(T_a = −40°C to + 85°C)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	UNIT
Data retention power supply voltage	V_{DDDR}		2.5		5.5	V
Data retention power supply current	I_{DDR}	V_{DDDR} = 2.5 V		1	15	μA
		V_{DDDR} = 5 V ±10%		15	50	μA
V_{DD} rise, fall time	t_{RVD} t_{FVD}		200			μs
$\overline{STOP}$ setup time to V_{DD}	t_{SSTVD}		12T +0.5			μs
$\overline{STOP}$ hold time from V_{DD}	t_{HVDST}		12T +0.5			μs

DATA RETENTION TIMING

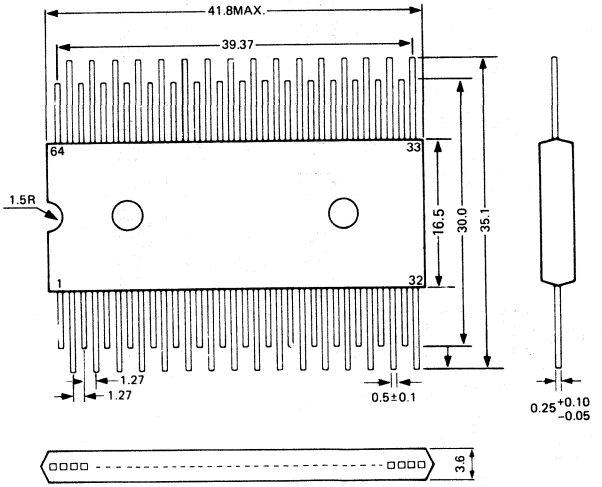


64 PIN PLASTIC
QUIP OUTLINE (Unit : mm)
μPD78C10G/μPD78C11G/μPD78C14G



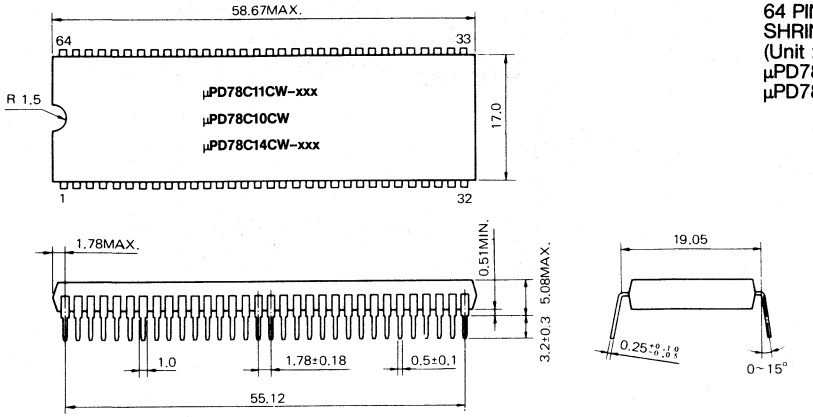
When ordering this package, specify as follows:
μPD78C10G-36
μPD78C11G-xxx-36
μPD78C14G-xxx-36

64 PIN PLASTIC
FLAT PACKAGE OUTLINE
(Unit : mm)
μPD78C11G/μPD78C14G

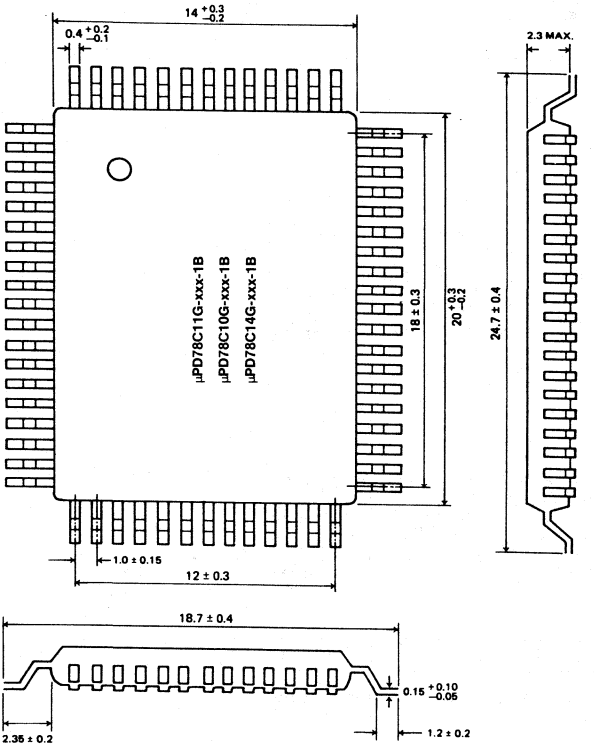


When ordering this package, specify as follows: μPD78C11G-XXX-37
μPD78C14G-XXX-37

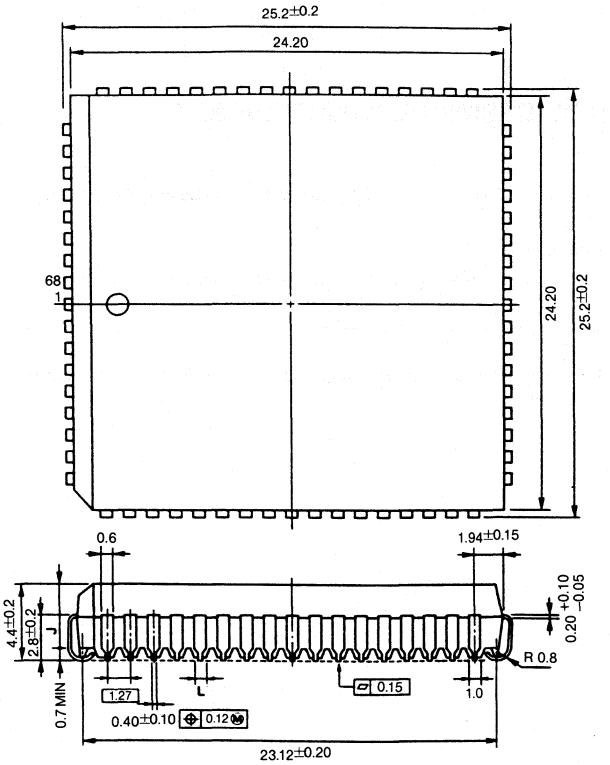
64 PIN PLASTIC
SHRINK DIP OUTLINE
(Unit : mm)
μPD78C10CW/C11CW
μPD78C14CW



64 PIN PLASTIC
FLAT PACK OUTLINE
(Unit : mm)
μPD78C10G/C11G
μPD78C14G



68 PIN PLASTIC LCC
PACKAGE OUTLINE
μPD78C10L/C11L/C14L



CMOS-DESIGN RECOMMENDATIONS

In order to maximize circuit reliability please note the general CMOS design rules.

For example:

1) Don't leave unused pins open, except they are outputs or no connected.

2) Never exceed the max. voltage range.

3) Avoid accurance of very fast voltage spikes or transission rate the power supply pin.

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